

VA30\_HB  
Schematics Document

UMA HDD NONTOUCH

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Title

Cover Page

Size

A3

Document Number

MA30 HB ULT

Date:

Tuesday, April 15, 2014

Sheet

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of

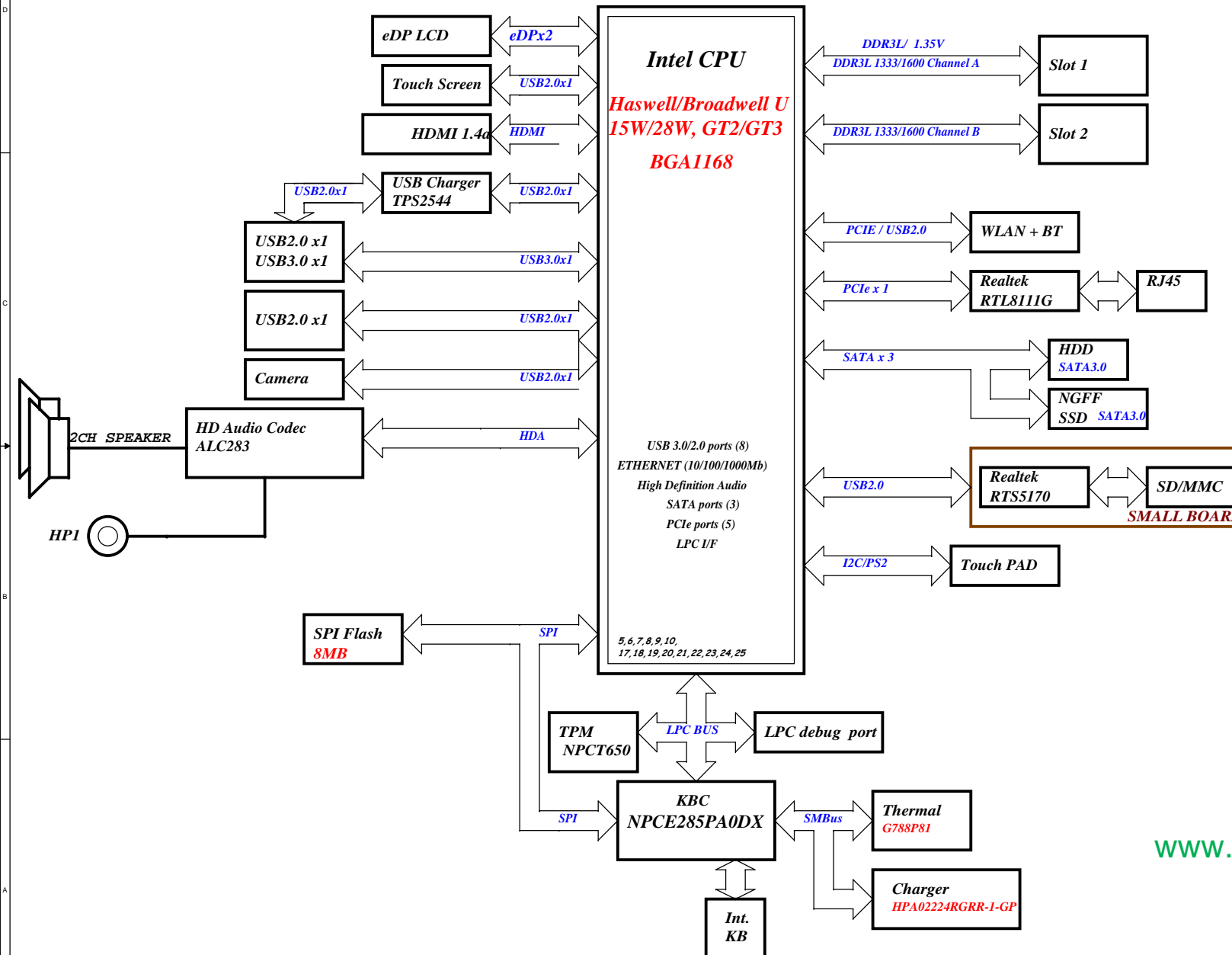
102

Rev

2

# VA30\_HB Board Block Diagram

Project code : 91.40Q01.001  
PCB P/N : 13334  
Revision : SA



[www.schematic-x.blogspot.com](http://www.schematic-x.blogspot.com)

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Title: <b>Block Diagram</b>			
Size Custom	Document Number	Rev SA	
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SSID = CPU

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Title

CPU (Reserved)

Size  
A3

Document Number  
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Rev  
SA

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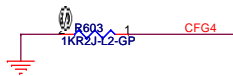
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SSID = CPU

eDP Enable	1:Disable
CFG4	0:Enable

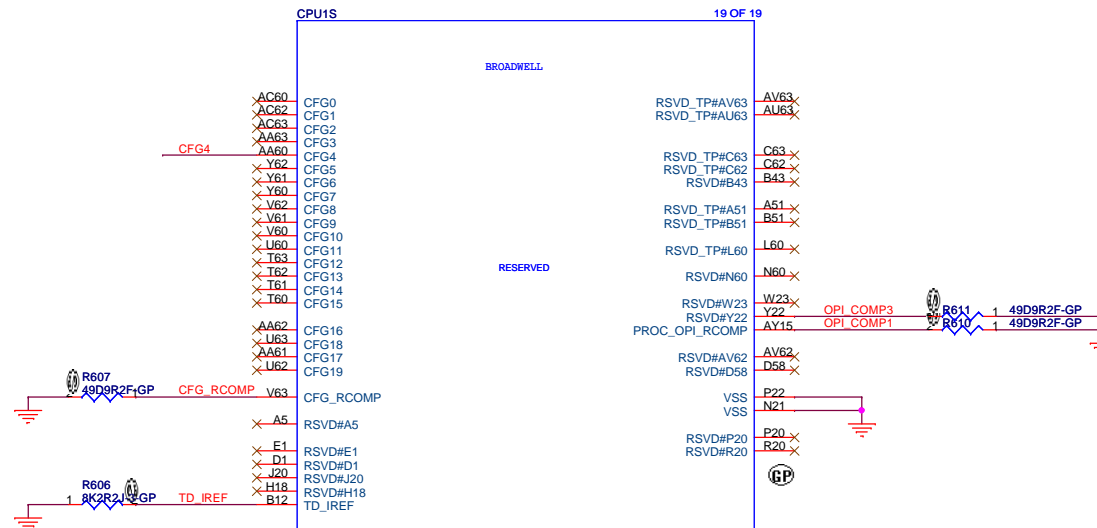


Signal Name	Description	Direction/Buffer Type
CFG[19:0]	<b>Configuration Signals:</b> The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. <ul style="list-style-type: none"><li>• <b>CFG[3:0]:</b> Reserved configuration lane. A test point may be placed on the board for these lanes.</li><li>• PCI Express* Static x16 Lane Numbering Reversal.</li><li>—</li><li>—</li><li>• <b>CFG[4]: eDP enable</b><ul style="list-style-type: none"><li>— 1 = Disabled</li><li>— 0 = Enabled</li></ul></li><li>• <b>[19:5]:</b> Reserved configuration lanes. A test point may be placed on the board for these lands.</li></ul>	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	
continued...		

## 7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD\_TP – these signals should be routed to a test point
- RSVD\_NCTF – these signals are non-critical to function and may be left un-connected

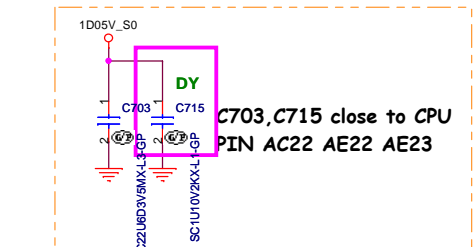
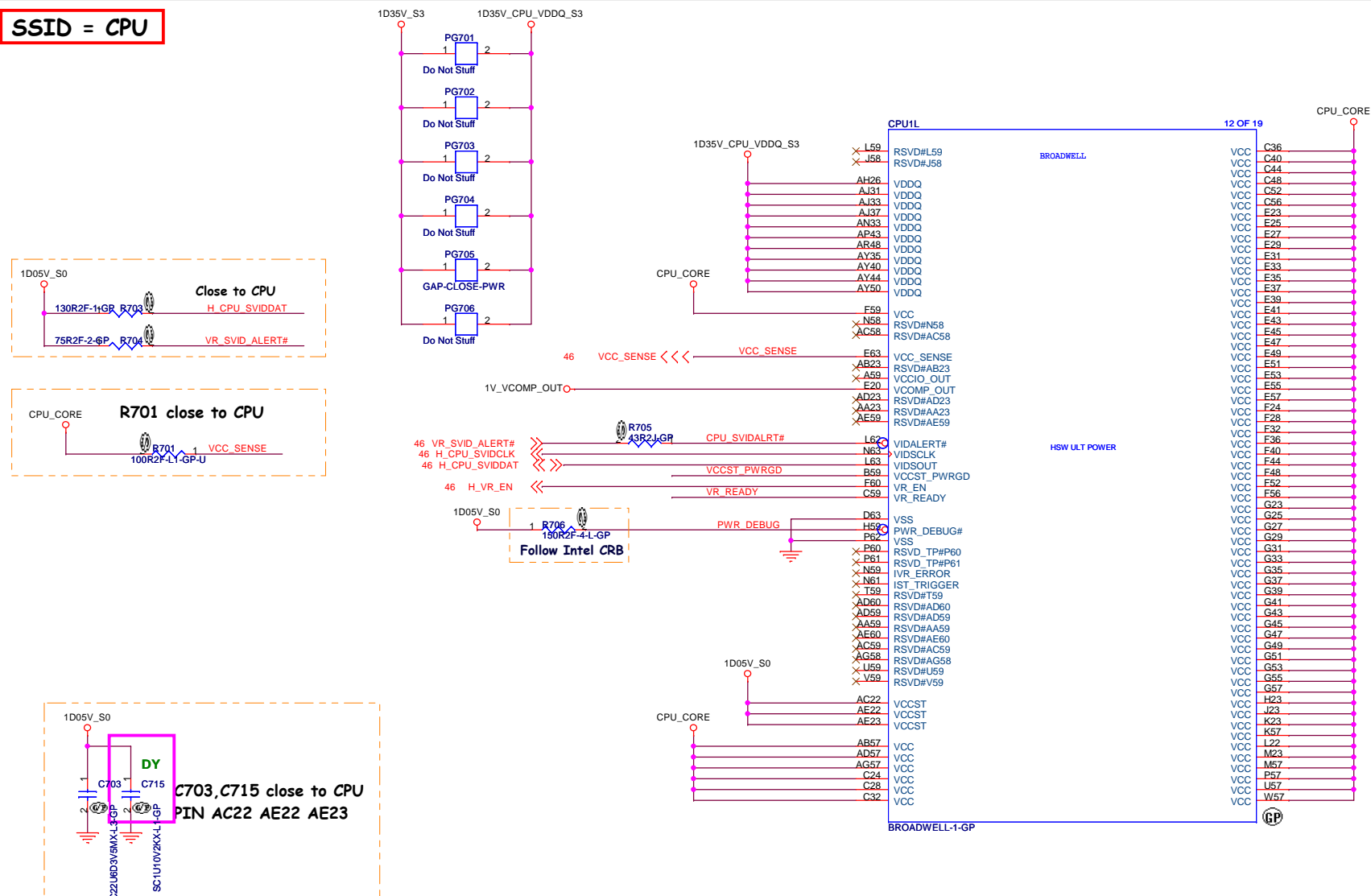


Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)	Default Value
CFG[0]		Connect a series 1 KΩ resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	Reserved. No connect		
CFG[4]	Display Port Presence strap	1:Disabled - No Physical Display Port attached to Embedded DisplayPort*, No connect for disable, 0:Enabled - An external Display Port device is connected to the Embedded Display Port. Pull-down to GND through a 1 KΩ ±5% resistor to enable port.	1
CFG[19:5]	Reserved configuration lands. A test point may be placed on the board for these lands.		

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Title			
CPU (CFG)			
Size Custom	Document Number	Rev	
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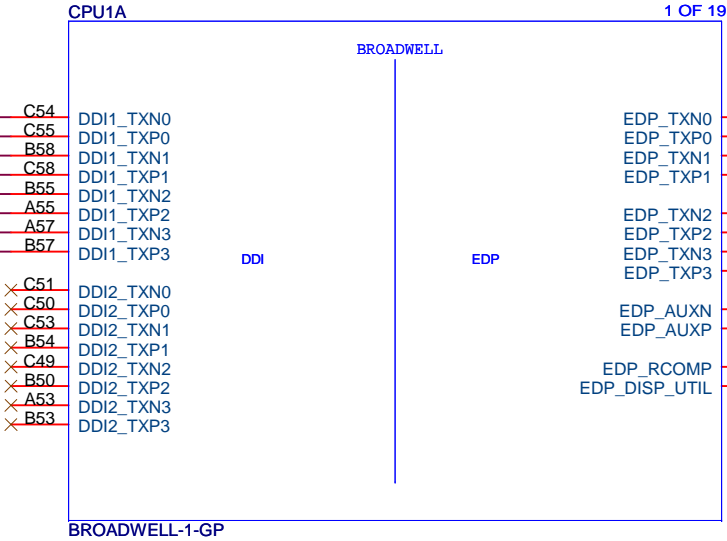
SSID = CPU



SSID = CPU

HDMI

54 HDMI\_DATA\_CPU\_N2 <<<  
54 HDMI\_DATA\_CPU\_P2 <<<  
54 HDMI\_DATA\_CPU\_N1 <<<  
54 HDMI\_DATA\_CPU\_P1 <<<  
54 HDMI\_DATA\_CPU\_N0 <<<  
54 HDMI\_DATA\_CPU\_P0 <<<  
54 HDMI\_DATA\_CPU\_N3 <<<  
54 HDMI\_DATA\_CPU\_P3 <<<



C45 EDP\_TX\_CPU\_N0 52  
B46 EDP\_TX\_CPU\_P0 52  
A47 EDP\_TX\_CPU\_N1 52  
B47 EDP\_TX\_CPU\_P1 52

eDP

C47  
C46  
A49  
B49

A45 EDP\_AUX\_CPU\_N 52  
B45 EDP\_AUX\_CPU\_P 52

D20  
A43



Layout Note:

Design Guideline:  
EDP\_COMP keep routing length max 100 mils.  
Trace Width:20 mils.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

Bit Rate	Supports (in # of lanes)	Peak Bandwidth
1.62 Gb/s	4	4 x 162 MB/s = 648 MB/s
5.4 Gb/s	4	4 x 540 MB/s = 2160 MB/s
2.7 Gb/s	4	4 x 270 MB/s = 1080 MB/s

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**CPU (DDI/EDP)**

Size

A4

Document Number

**MA30 HW ULT**

Date

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1

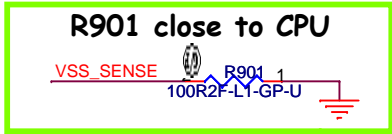
Rev

**SA**

102



**SSID = CPU**



## Layout Note:

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### CPU (VSS)

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# MA30 HB ULT

Date: Tuesday, April 15, 2014

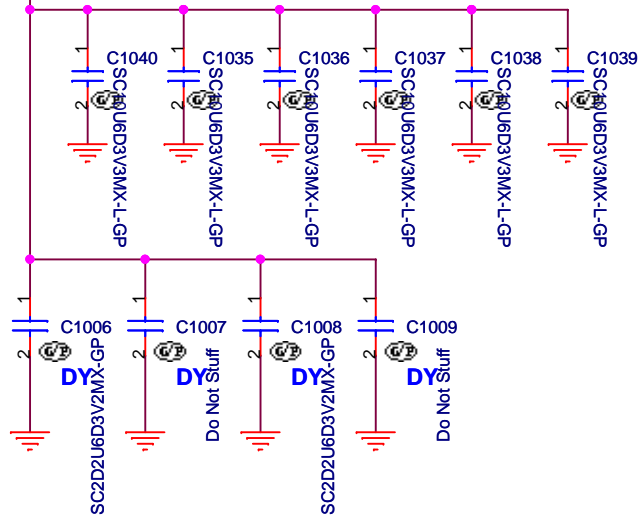
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V

SA

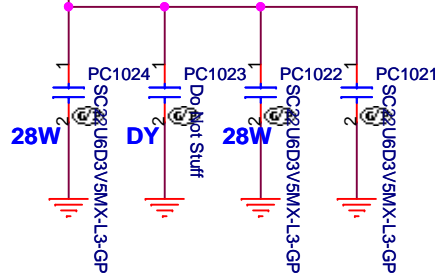
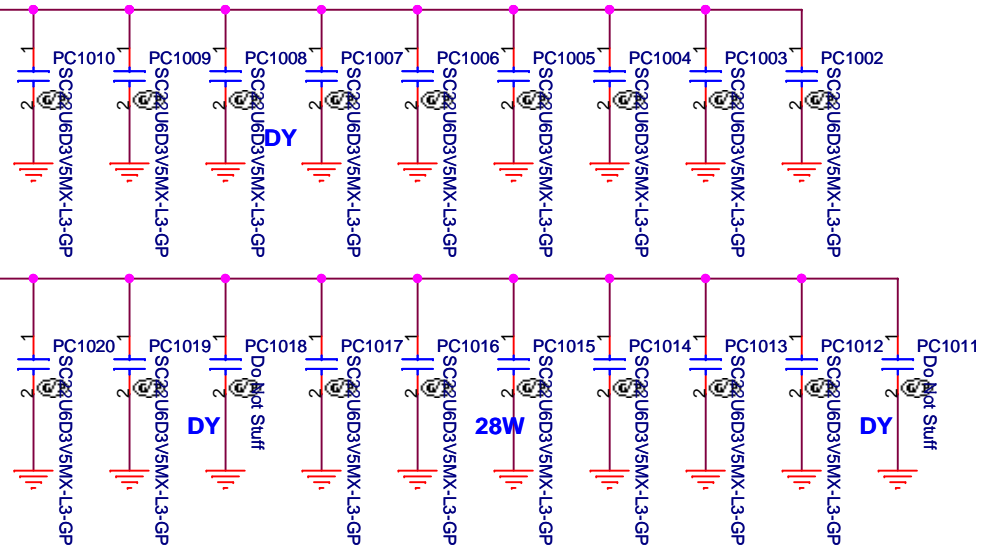
2

1D35V\_CPU\_VDDQ\_S3



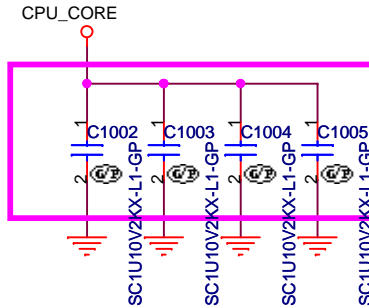
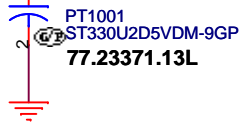
For Intel Recommend EE Part

CPU\_CORE



CPU\_CORE

28W



For Intel Recommend EE Part

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Title

CPU (Power CAP1)

Size

A4

Document Number

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Rev

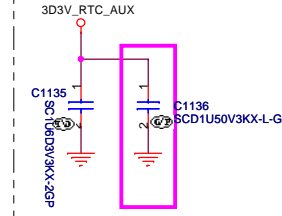
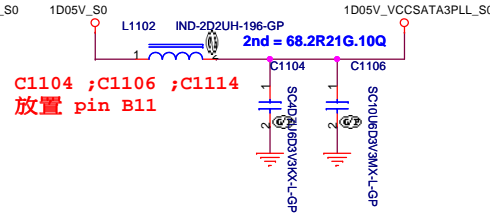
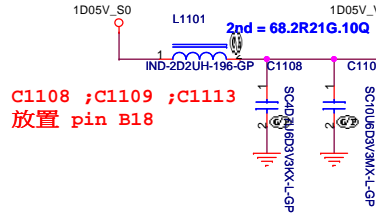
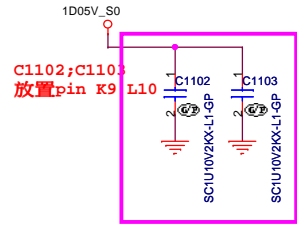
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Date: Tuesday, April 15, 2014

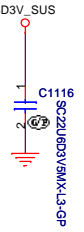
Sheet 10 of 102

0726\_SA 擺放電容的位置請參考Page 21  
每個位置如下

MAX: 1.92A

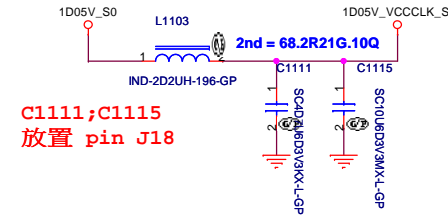
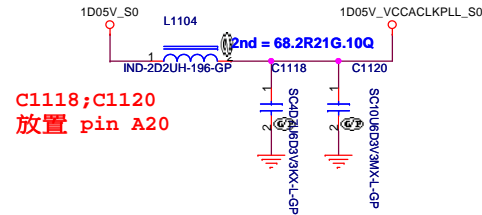
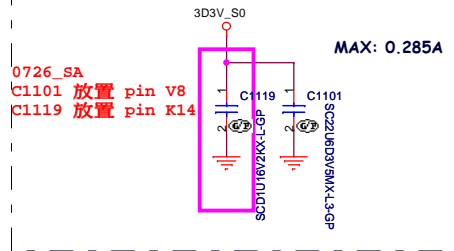


C1116放置 pin AC9

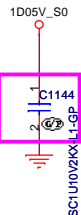


0726\_SA  
C1135;C1136  
放置 pin AG10

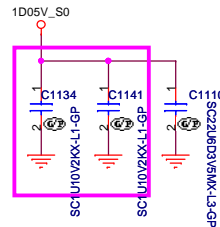
MAX: 3.51A



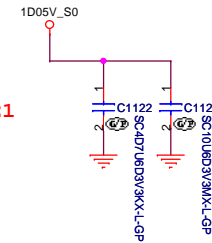
C1144  
放置 pin AE9



C1110 放置 pin J11  
C1134 C1141 放置 pin J11, AE8



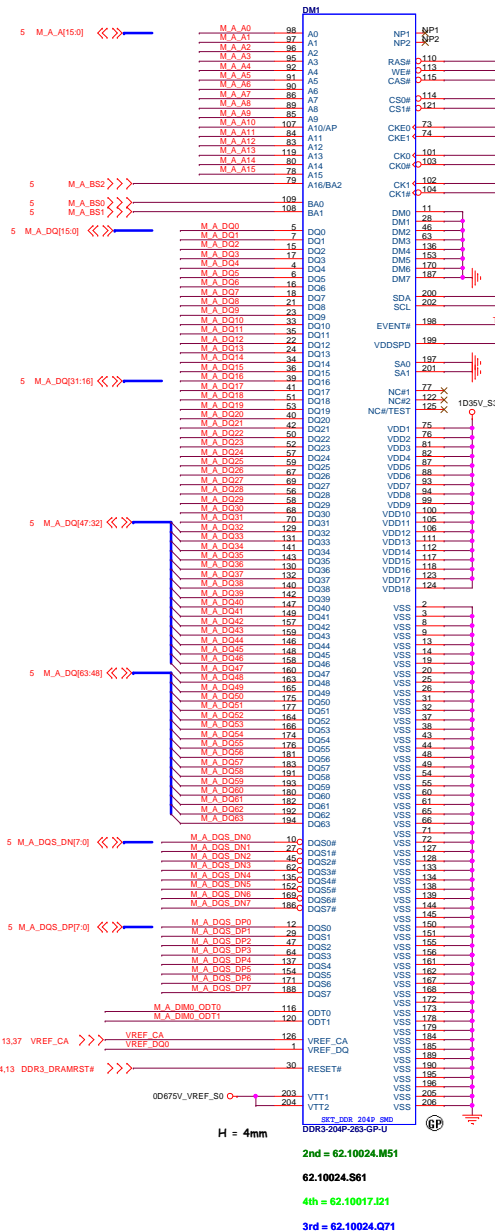
C1122;C1123  
放置 pin AA21



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Title			
<b>CPU (Power CAP2)</b>			
Size	Document Number	Rev	
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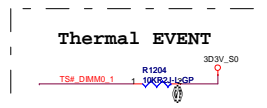
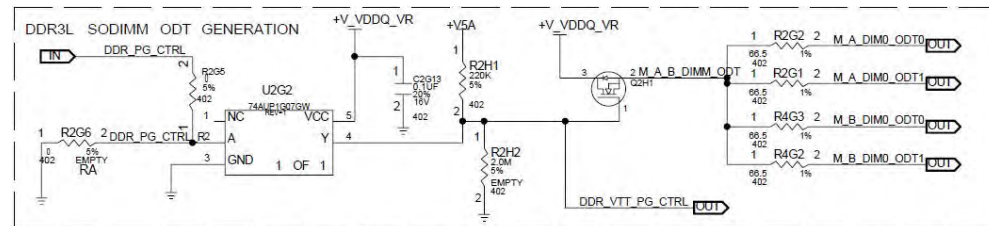
## SSID = MEMORY



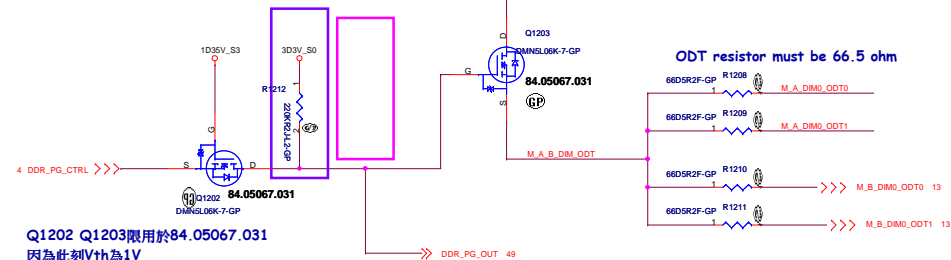
**Note:**  
If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30

If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32

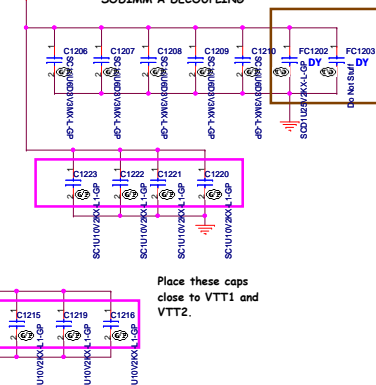
**SODIMM Memory Connectivity and Topology**  
**ODT Signal Connectivity and Support**  
 For DDR3L SODIMM designs, Intel recommends ODT signals not to be routed between CPU and DIMM on platform, leave ODT at CPU as no-connect (open), and tie DIMM ODT to VDDIO through FET and resistor. The reason for this additional ODT-control is that the ODT signal is not needed for DDR3L SODIMM. The VTT path is not needed during low power states, as ODT signal is terminated to VTT through RTT on SODIMM. The ODT value for DDR3L SODIMM 1-1PC platform will be encoded in the write command and use RCTR\_M0M\_0 and RCTR\_M0E\_0 (60-120 Ohm).  
 \* CPU ODT output would be NOCON  
 \* SODIMM ODT input should be tied to VDDIO through a FET and a resistor to support low power state



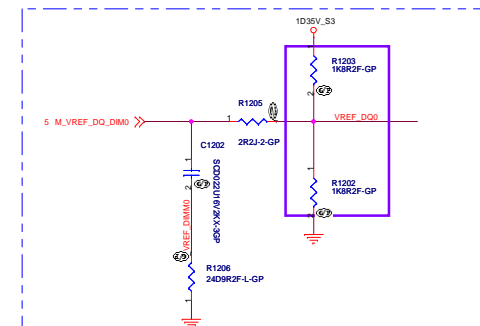
Layout Note:  
Place these Caps near  
SO-DIMMA.



## SODIMM A DECOUPLING



Place these caps  
close to VTT1 and  
VTT2.



For Intel Recommend Close to DIMM

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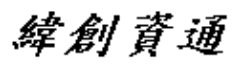
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<b>DDR3-SODIMM1</b>			
Size	Document Number		Rev
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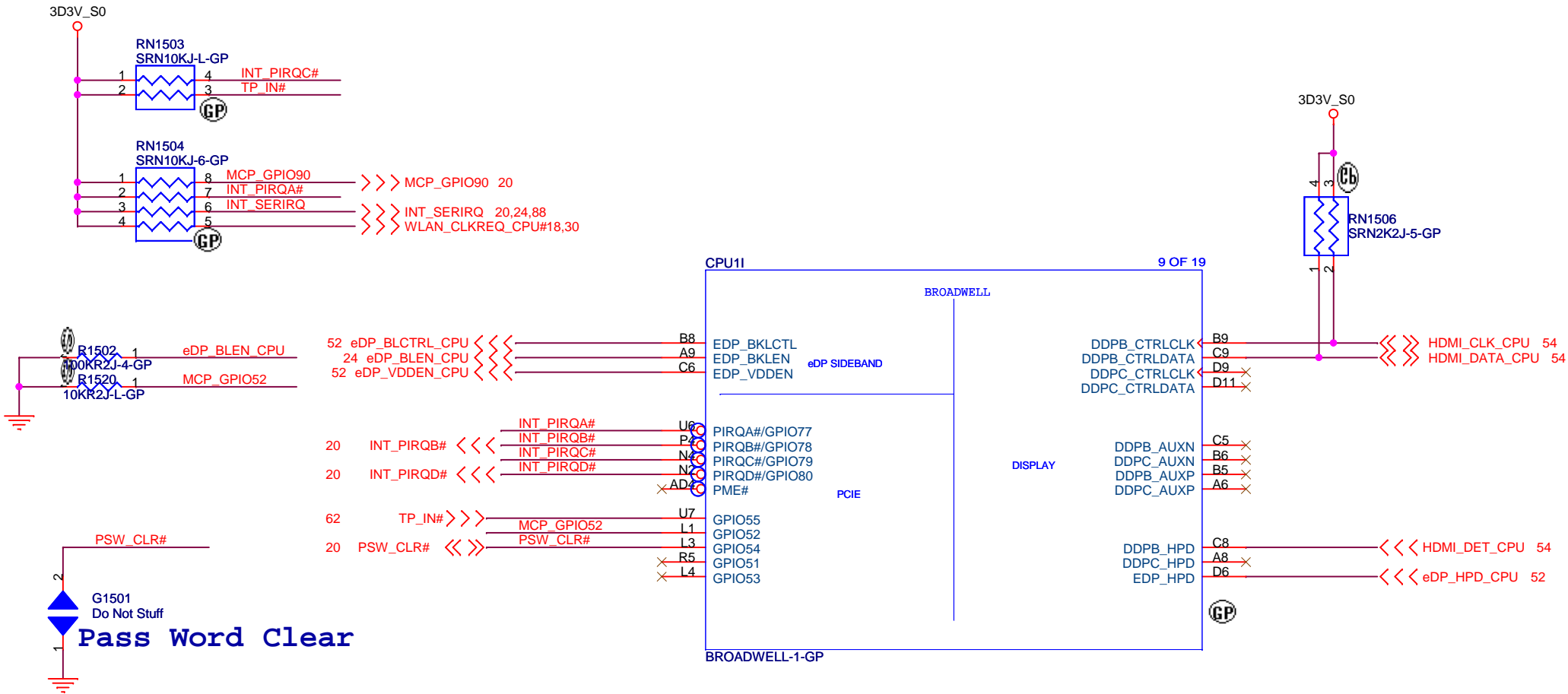
5	4	3	2	1
D				
C				
B				
A				

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Title <b>(Reserved) _SODIMM_ SODIMM4</b>			
Size A4	Document Number <b>MA30 HB ULT</b>		Rev <b>2</b>
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SSID = CPU



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Title

**CPU(EDP SIDE BAND/GPIO/DDI)**

Size

A4

Document Number

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Rev

**2**

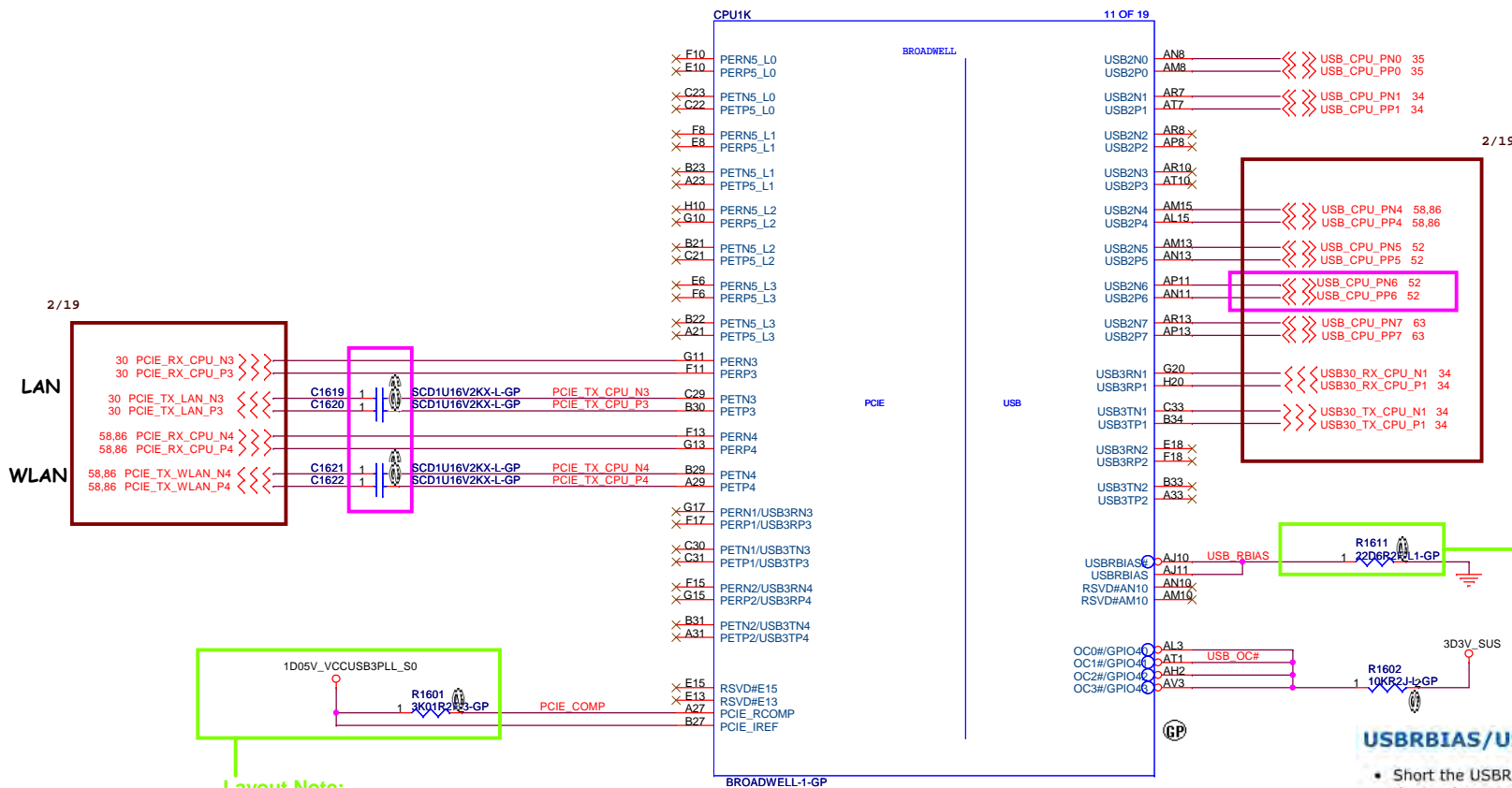
Date: Tuesday, April 15, 2014

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**SSID = PCH**

## USB Table

Pair	Device
0	USB2.0 Port 1
1	USB3.0 Port 2(USB2.0)
2	
3	
4	WLAN(Bluetooth)
5	Touch screen
6	CCD
7	Card reader



- **Layout Note:**

1. USB\_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

## USBRBIAS/USBRBIAS# Connection Guidelines

- Short the USBRBA5 and the USBRBA5# pins at the package and then route on the top layer to one end of a  $22.6\ \Omega \pm 1\%$  resistor to ground (see [Figure 15-2](#)).
- Route signal using 50 ohm single-ended impedance and 500 mils (12.7-mm) max trace length and no longer than 450 mils to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

**Layout Note:**

1. PCIe\_RCOMP/ PCIe\_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

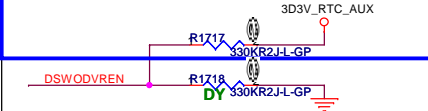
Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) <b>Note:</b> Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) <b>Note:</b> Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils



SSID = PCH

Bit	Description
31:3	Reserved
2	<b>WAKE# Pin Deep Sx Enable (WAKE_PIN_DSX_EN)</b> - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': <ul style="list-style-type: none"><li>Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time.</li><li>Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled.</li></ul> <b>NOTE:</b> Deep Sx disabled configuration must leave this bit at '0'.

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



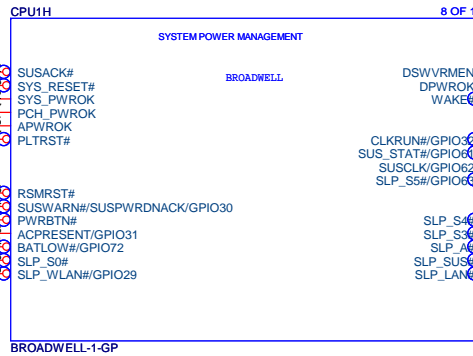
-1 04/08  
24 S0\_PWR\_GOOD  
36 PCH\_PWROK  
24,30,36,58,65,86,88 PLT\_RST# <<<

1 R1724 2  
Do Not Stuff

24 PM\_SUSACK# >>>  
-1 04/08  
1 R1729 2  
Do Not Stuff

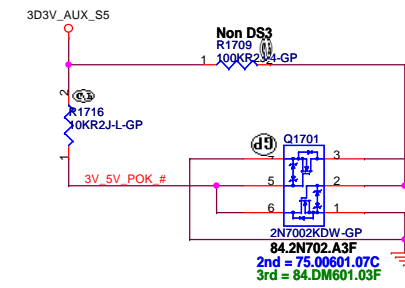
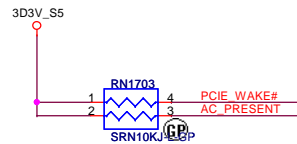
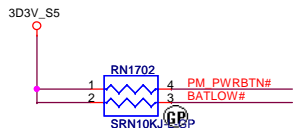
24 PM\_SUSWARN# >>>  
24,86 PM\_PWRBTN# >>>  
24 AC\_PRESENT >>>

PM\_SUSACK# AK2  
SYS RESET# AC2  
SYS\_PWROK R AC2  
AY7  
AB5  
APWROK  
PLTRST#

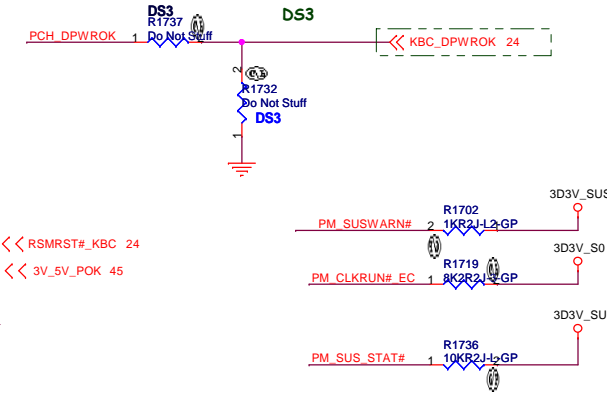


DSWVRMEN AW7  
DPWROK AV5  
WAKE# AJ5  
CLKRUN#/GPIO30 CV5  
SUS\_STAT#/GPIO6 AG4  
SUSCLK#/GPIO6 AE6  
SLP\_S5#/GPIO6 AF5  
SLP\_S4# AJ6  
SLP\_S3# AT4  
SLP\_SUS# AL5  
SLP\_LAN# AP4

DSWODVREN 1  
PCH\_DPWROK 1  
PM\_RSMRST# <<<  
PCIE\_WAKE# 24,30,58  
PM\_CLKRUN#\_EC 24,88  
PM\_SUS\_STAT# 88  
SUS\_CLK\_CPU 58  
PM\_SLP\_S4# 24,49  
PM\_SLP\_S3# 24,36,48,51  
PM\_SLP\_SUS# 24,38



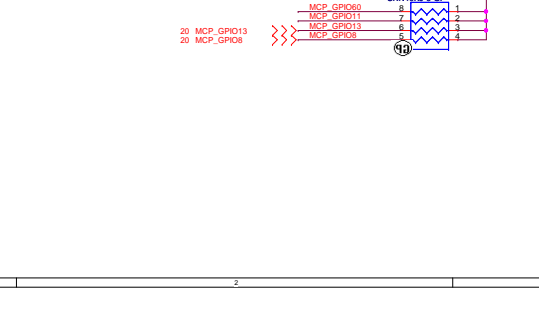
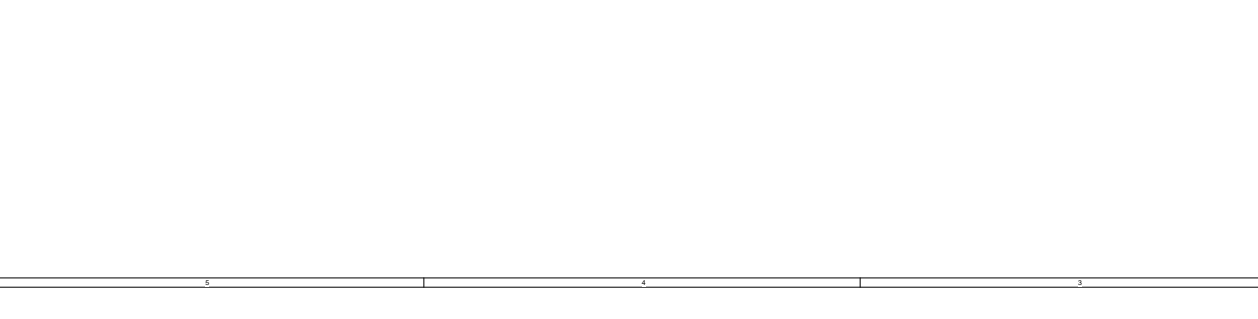
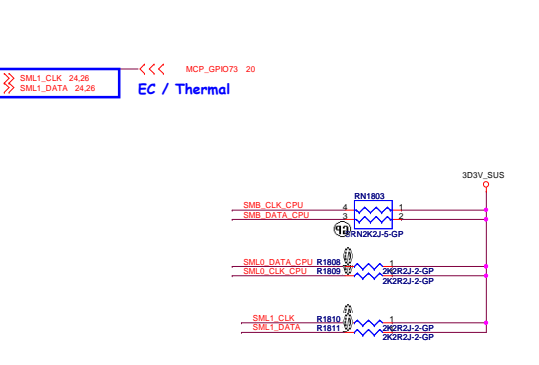
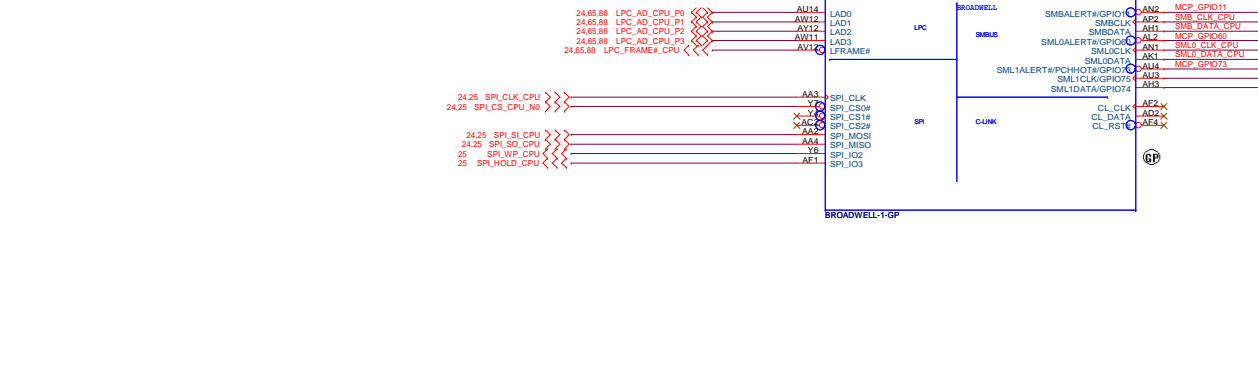
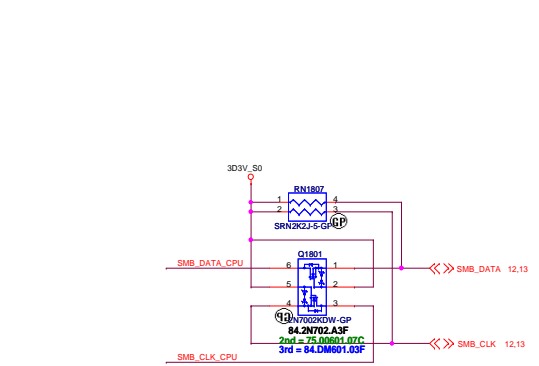
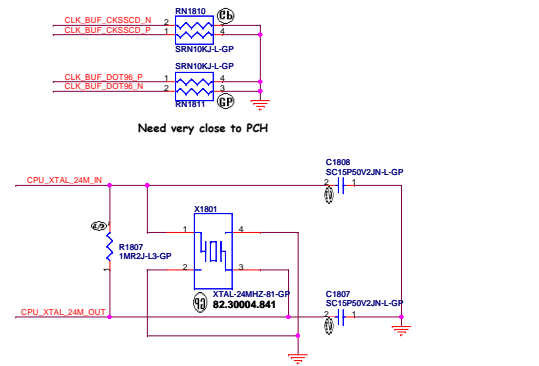
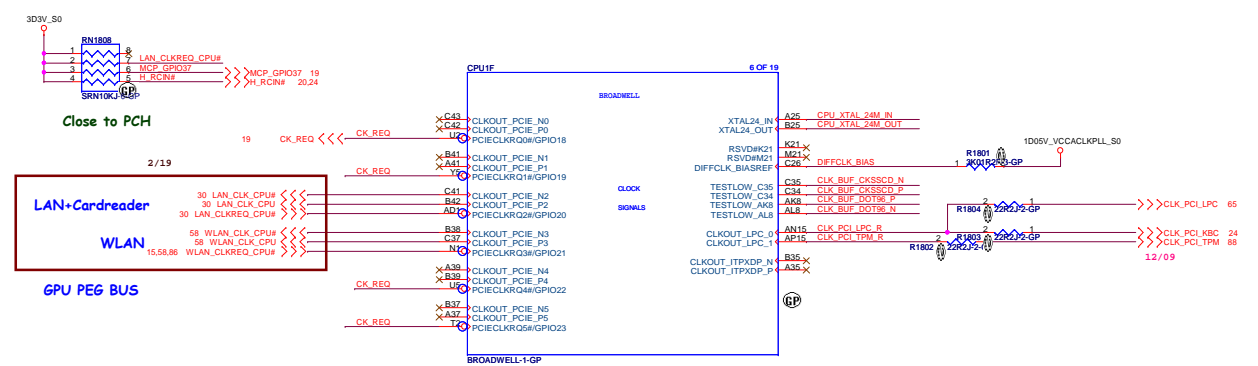
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RSMRST#\_KBC 24  
3V\_5V\_POK 45  
PM\_SLP\_SUS# <<<



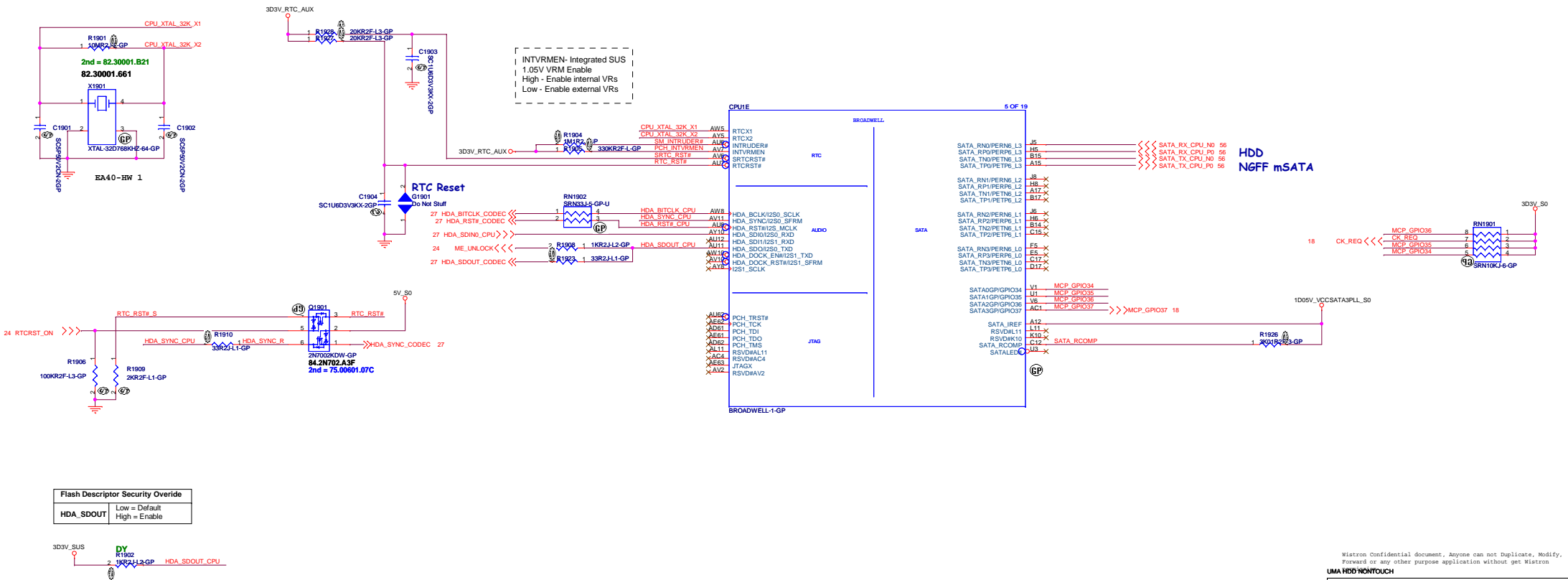
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File CPU (DMI/FDI/PM)	
Size A3	Document Number MA30 HB ULT
Date: Tuesday, April 15, 2014	Sheet 17 of 102

SSID = PCH



**SSID = PCH**



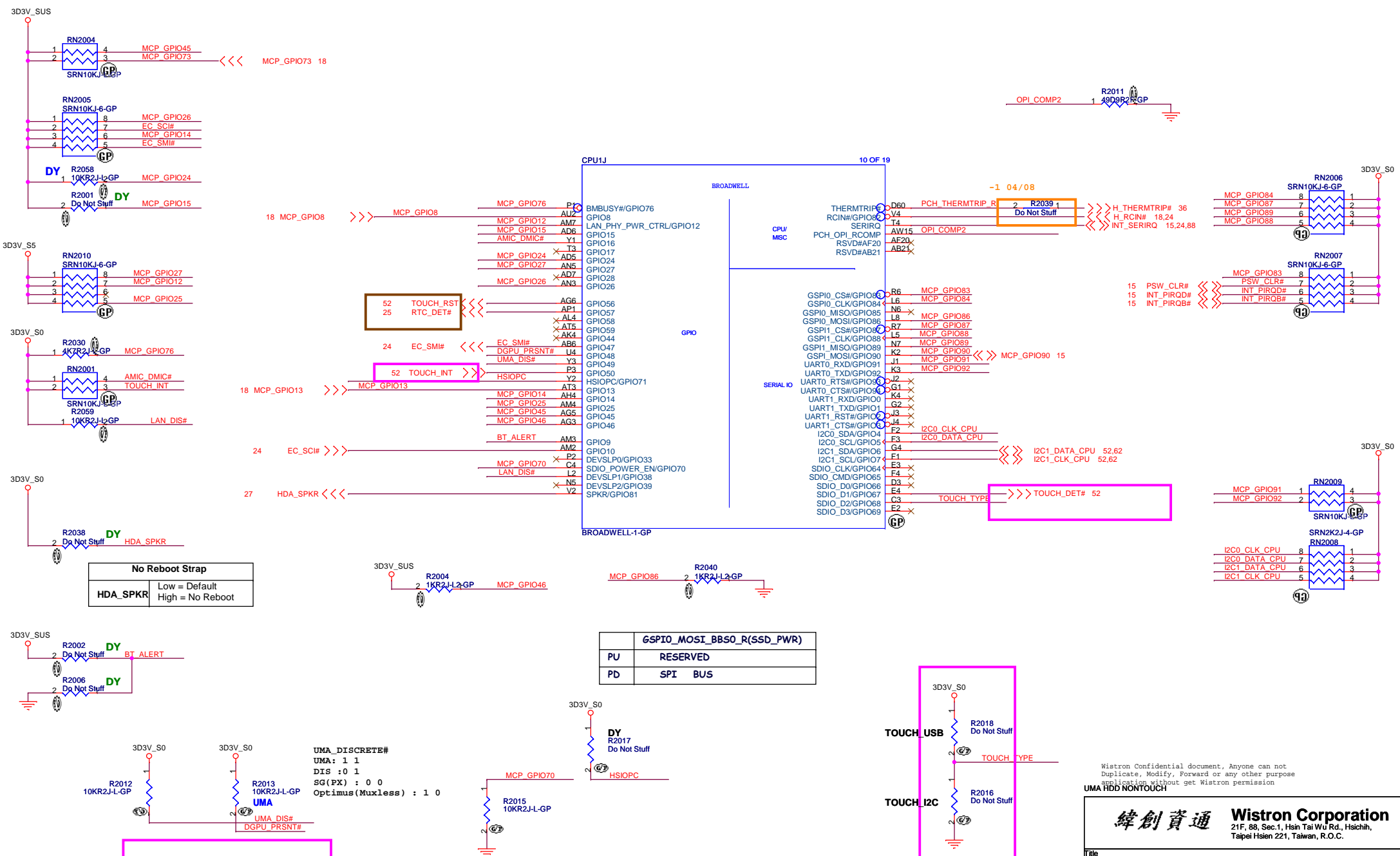
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Title			
<b>CPU (RTC/LPC/SATA/HDA)</b>			
Size	Document Number	Rev	
Custom	<b>MA30 HB ULT</b>	<b>2</b>	
Date:	Tuesday, April 15, 2014	Sheet	19 of 102

**SSID = PCH**



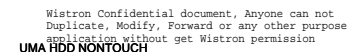
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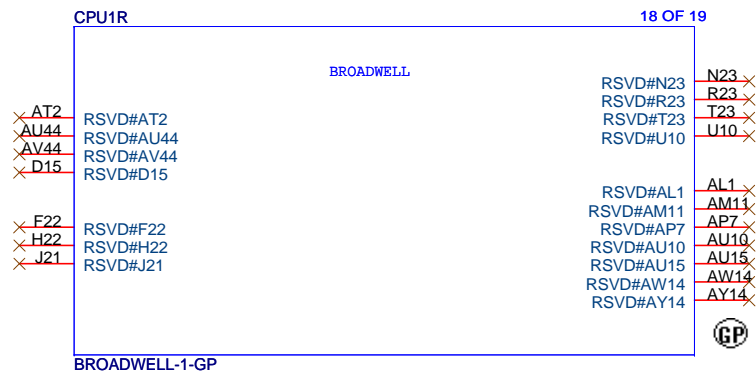
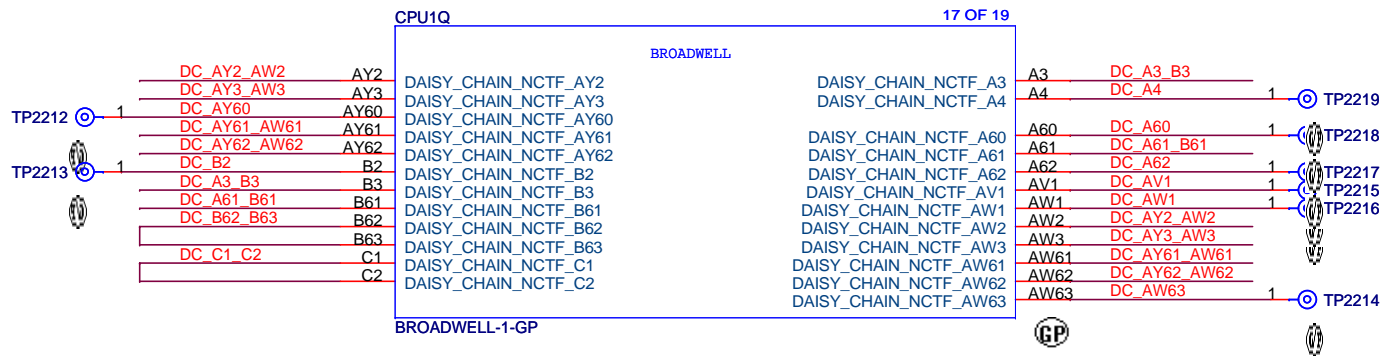
Title			
<b>CPU (GPIO/MISC)</b>			
Size A3	Document Number		Rev
	<b>MA30 HB ULT</b>		<b>2</b>
Date:	Tuesday, April 15, 2014	Sheet 20 of	102

1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to [Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.](#)



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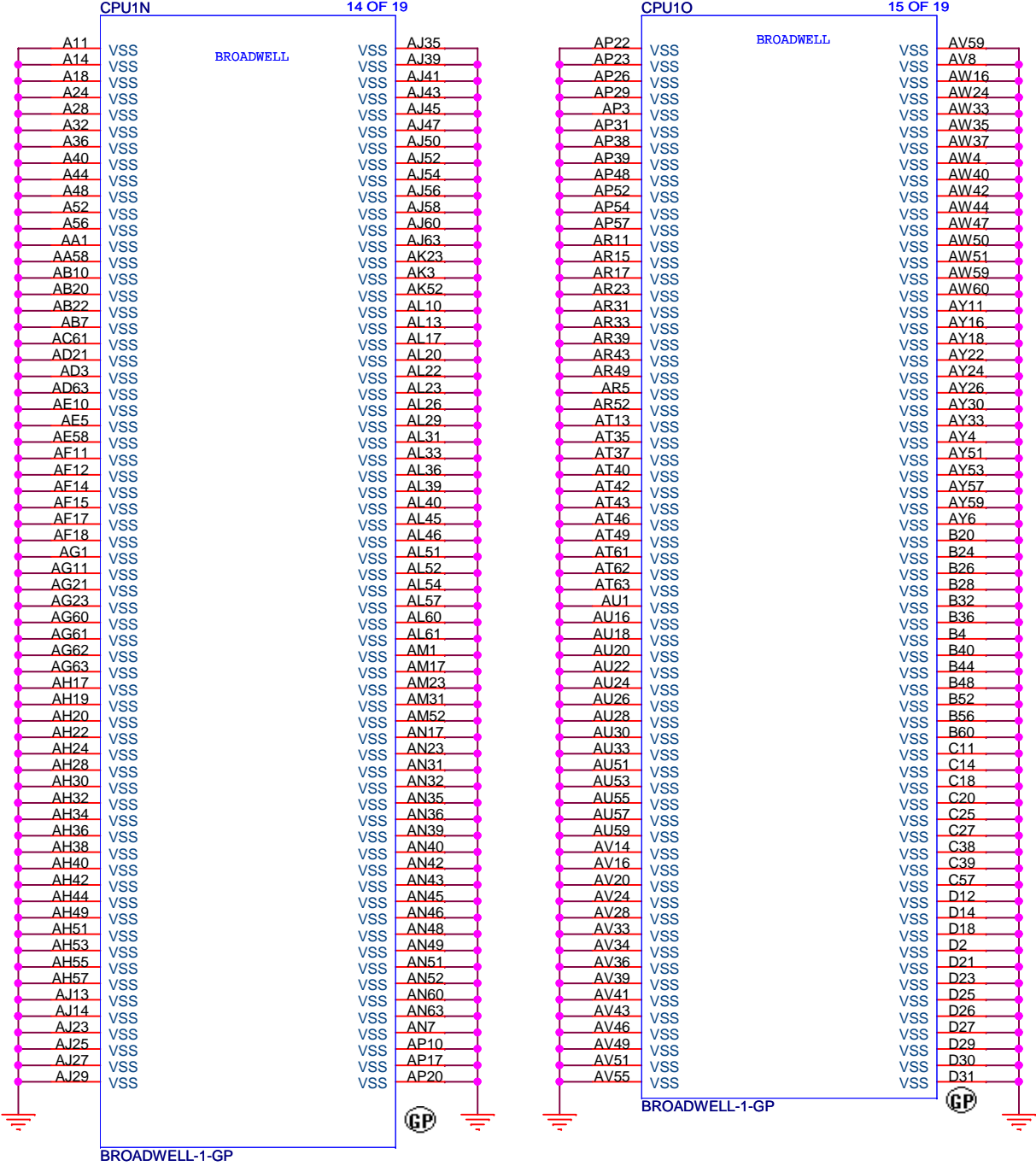
Title			
<b>CPU (POWER1)</b>			
Size A3	Document Number		Rev
	<b>MA30 HB ULT</b>		<b>2</b>
Date:	Tuesday, April 15, 2014	Sheet 21 of	102




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Title			
CPU (RSVD)			
Size	Document Number		Rev
Custom	MA30 HB ULT		2
Date:	Tuesday, April 15, 2014		Sheet 22 of 102

SSID = PCH



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			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>CPU (VSS)</b>					
Size A4	Document Number <b>MA30 HB ULT</b>				Rev <b>2</b>
Date: Tuesday, April 15, 2014		Sheet 23		of 102	



PCR_Ver_A0	Pu-Low Register	Pu-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.875 V
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408	>= 2.616 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V
-I	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.894 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>= 1.758 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	>= 1.281 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	>= 0.924 V



Period 1	Period 2	Period 3	Period 4	Period 5	Period 6	Period 7	Period 8



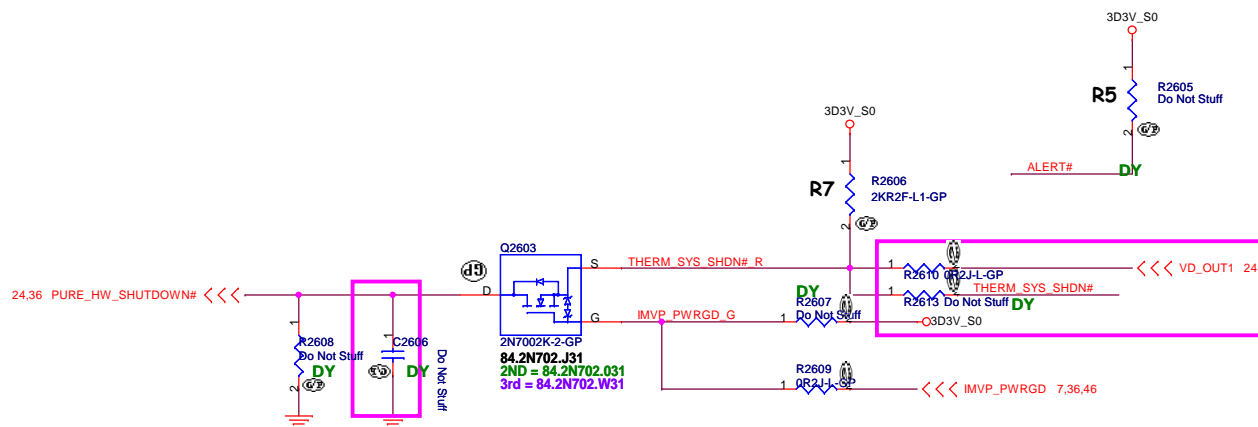
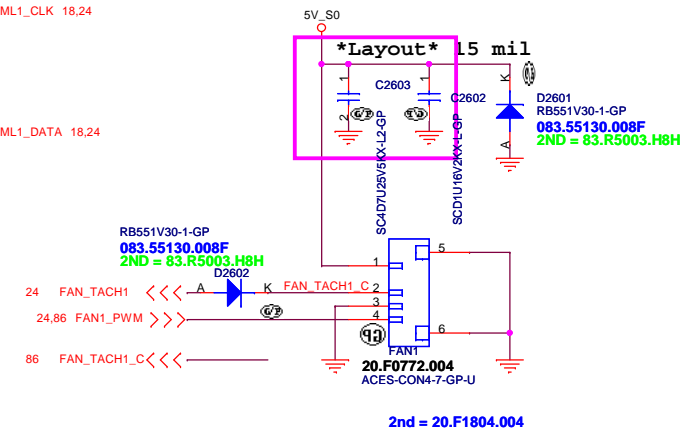
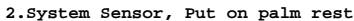


**SPI FLASH ROM (8M byte) for PCH**

SPI Socket for LAB stage

Title			
<b>Flash/(KBC+PCH)/RTC</b>			
Size A2	Document Number		Rev
	<b>MA30 HB ULT</b>		<b>2</b>
Date:	Tuesday, April 15, 2014	Sheet 25 of	102

***Thermal sensor NCT 7718W***



ALERT# /T CRIT#  
Pull-up R̄esistor

	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5					
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T CRIT temperature strapping point

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Title			
<b>G788P81/Fan Controllor P2793</b>			
Size	Document Number		Rev
A3		<b>MA30 HB ULT</b>	<b>S</b>
Date:	Tuesday, April 15, 2014	Sheet 26 of	102

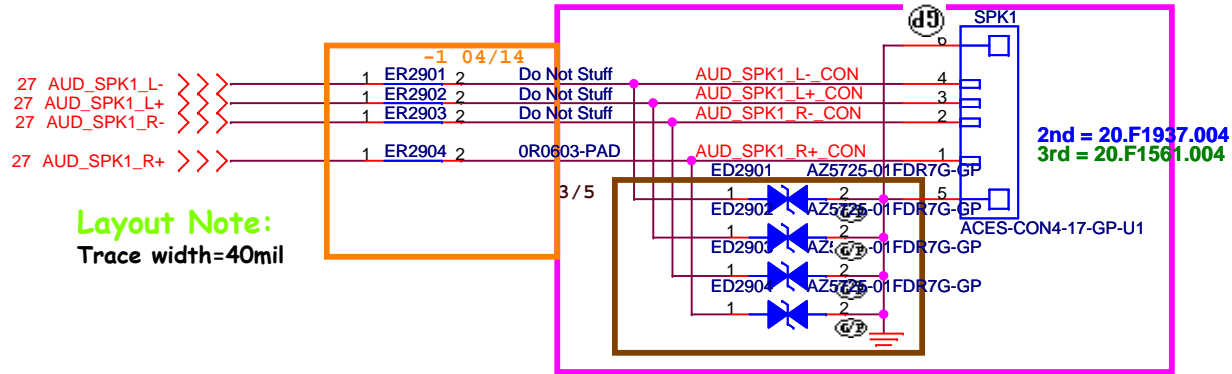


5	4	3	2	1
D				D
C				C
B				B
A				A

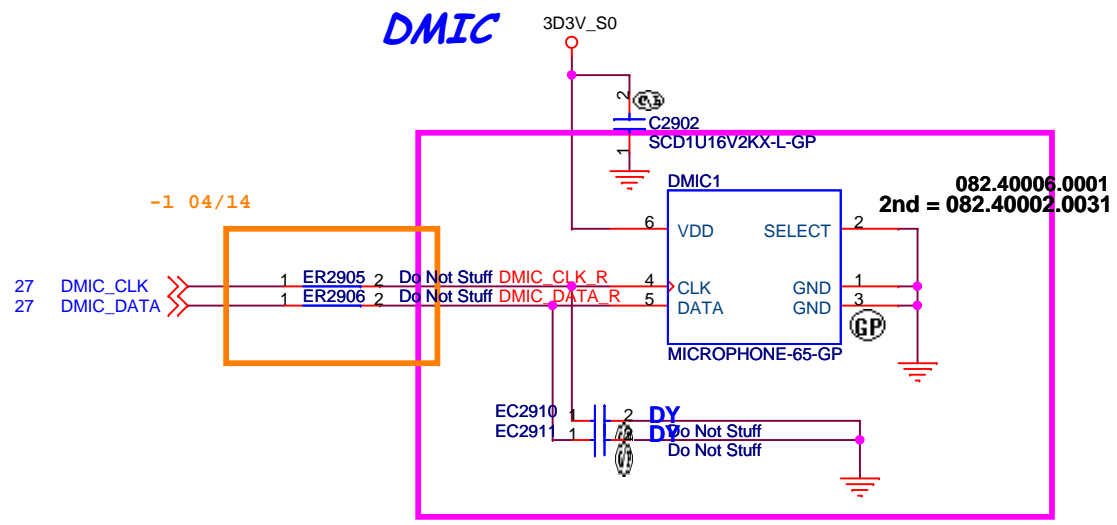
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Title		
Audio AMP 1001		
Size	Document Number	Rev
A4	MA30 HB ULT	SA
Date:	Tuesday, April 15, 2014	Sheet 28 of 102



Layout Note:  
 Trace width=40mil



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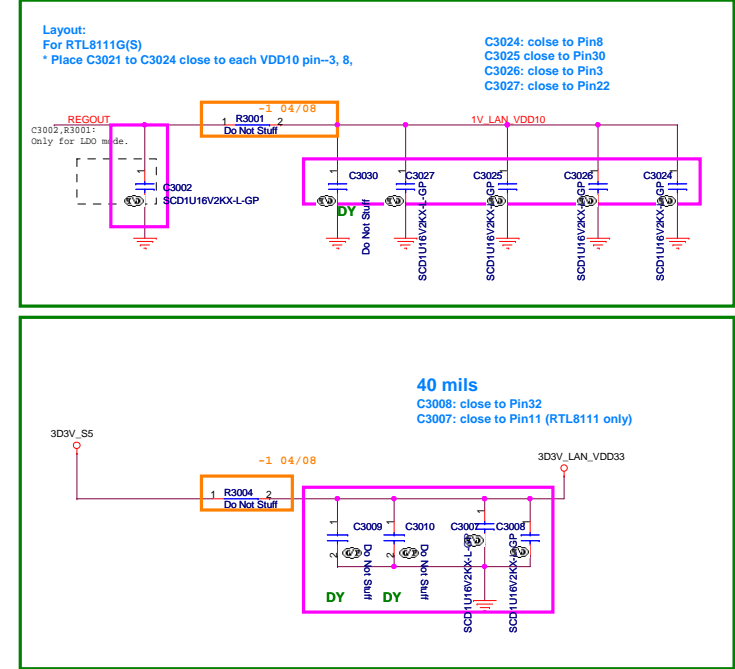
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Title  
**Audio Jack**

Size A4 Document Number **MA30 HB ULT** Rev **SA**

Date: Tuesday, April 15, 2014 Sheet 29 of 102

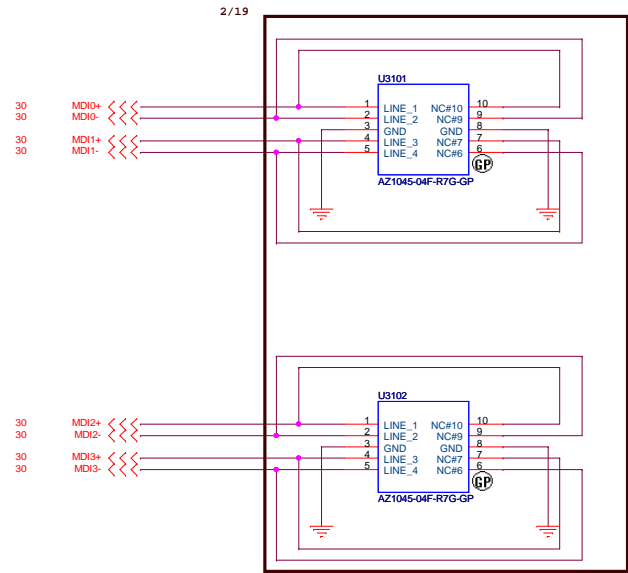
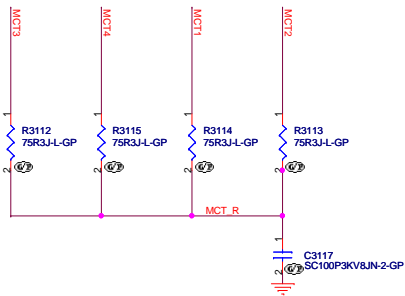
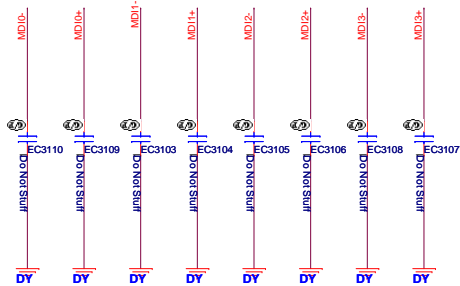
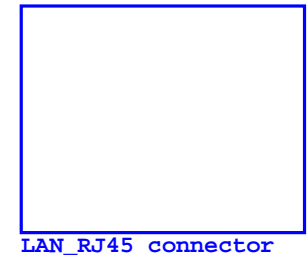
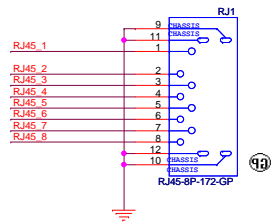
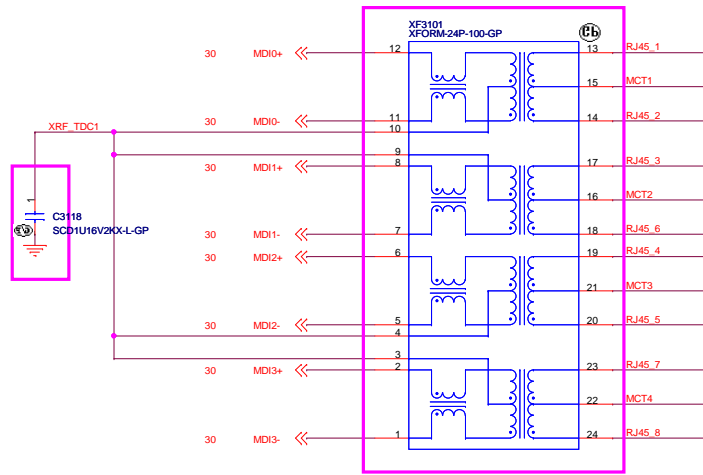


application with  
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Title			
<b>LAN(RTL8411)</b>			
Size	Document Number	Rev	
Custom	<b>MA30 HB ULT</b>	<b>2</b>	
Date:	Tuesday, April 15, 2014	Sheet 30 of	102

SSID = LAN



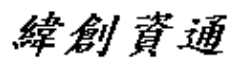
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<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>(LAN+VGA) CONNECTOR</b>			
Size	Document Number	Rev	
Custom		<b>2</b>	
<b>MA30 HB ULT</b>			
Date:	1/8/2014, April 15, 2014	Sheet	31 of 102

5	4	3	2	1
D				D
C				C
B				B
A				A

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Title <b>RTS5229(CARD READER)</b>		
Size A4	Document Number <b>MA30 HB ULT</b>	Rev <b>2</b>
Date: Tuesday, April 15, 2014		Sheet 32 of 102



SSID = SDIO

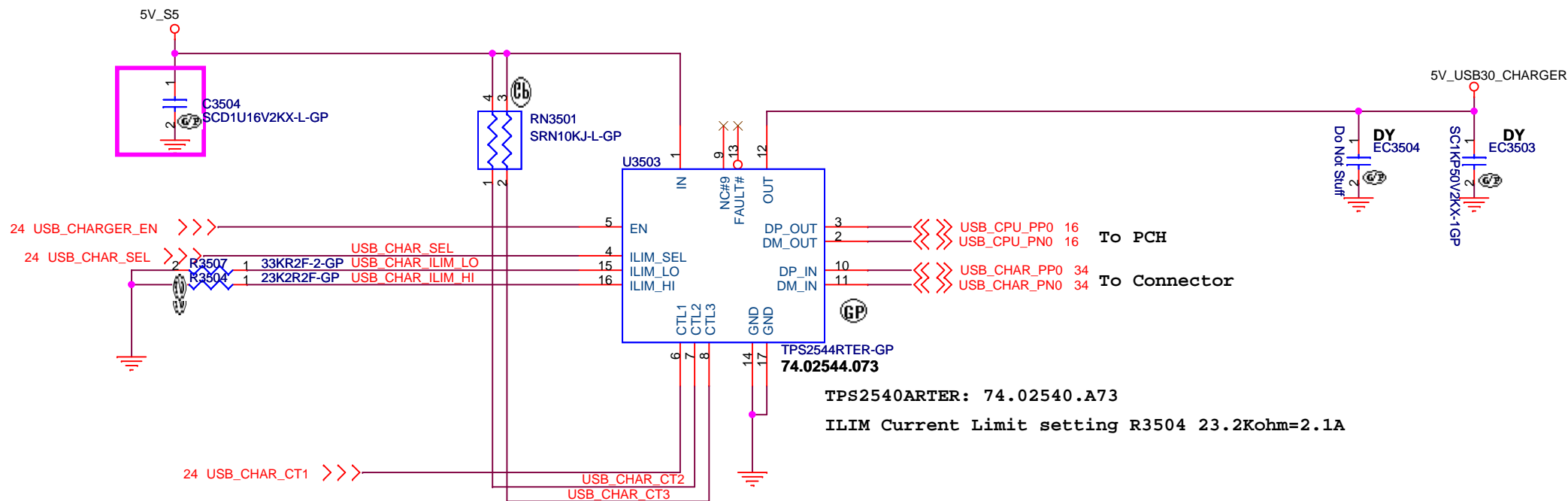
# SD//MS Card Reader

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Title			
CARD Reader CONN			
Size	Document Number		Rev
Custom	MA30 HB ULT		2
Date:	Tuesday, April 15, 2014		Sheet 33 of 102





### 3. Electrical Safety for USB3.0 Port

2.0 A  $\leq$  Measurement value  $\leq$  2.2 A : Pass

1.9 A  $\leq$  Measurement value  $<$  2.0 A or 2.2 A  $<$  Measurement value  $\leq$  2.4 A : Marginal

If this result is "Marginal", 4 more samples (Total 5 samples) must be measured for each port.

And it must be confirmed that the values of 5 samples can meet our requirement (1.9 A - 2.4 A).

### Device Control Pins

Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	0	1	0
	0	1	1	X

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Title

**USB CHARGER**

Size  
A4

Document Number

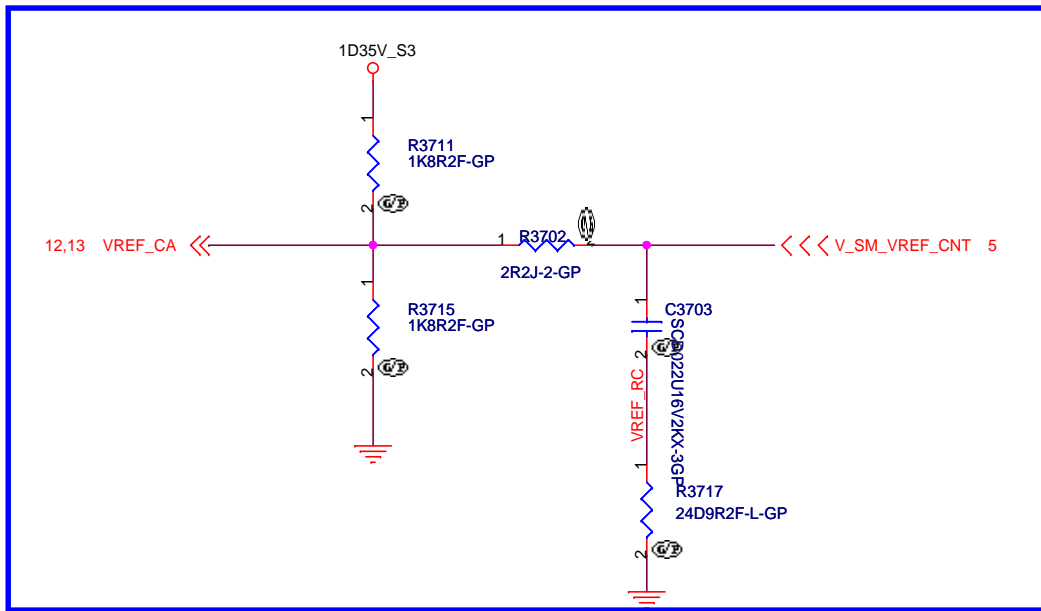
**MA30 HB ULT**

Rev  
SA

Date: Tuesday, April 15, 2014

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For Intel Recommend Close to DIMM

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Title	
<b>ADAPTER OCP / S3 reduction</b>	
Size	Document Number
Custom	<b>MA30 HB ULT</b>
Date:	Tuesday, April 15, 2014
Sheet	37 of 102
Rev	<b>2</b>



Power Sequence

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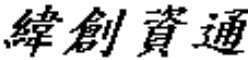
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緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
1D05 M			
Size	Document Number		Rev
Custom	MA30 HB ULT		2
Date:	Tuesday, April 15, 2014		Sheet 39 of 102

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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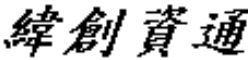
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Connected Standby1</b>			
Size A	Document Number <b>MA30 HB ULT</b>		Rev <b>2</b>
Date: Tuesday, April 15, 2014	Sheet	40	of 102



5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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Title			
<b>Connected Standby2</b>			
Size A	Document Number <b>MA30 HB ULT</b>		Rev <b>2</b>
Date: Tuesday, April 15, 2014	Sheet	41	of 102

## Adaptor in to generate DCBATOUT

PC4201  
SCD1U50V3KX-L-GP

83.P6SMB.AAG  
2nd = 083.00020.00AG  
3rd = 83.P6SMB.EAG

AD\_JK

PD4203  
P6SMB

PC4202  
SC1U50V5ZY-1-GP-U

PU4201  
TPCC8131-GP  
**84.07129.037** AD  
**2nd = 84.08131.037**

AD+

EC4205  
Do Not Stuff  
DY

PWR\_AD+\_2

PR4202  
100KR2J-4-GP

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Title
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***DCIN JACK***

Size  
A4

Document Number

# MA30\_HB ULT

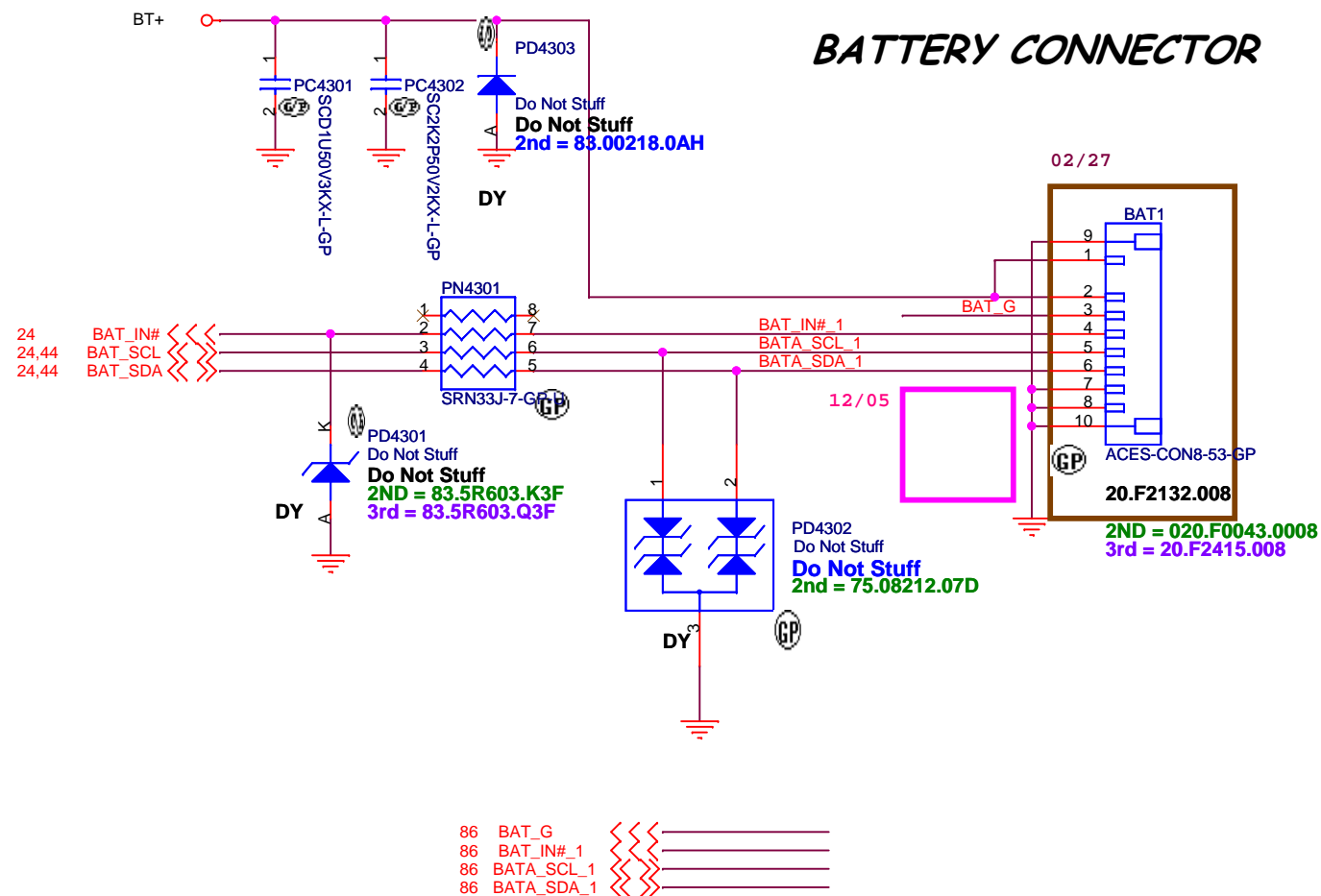
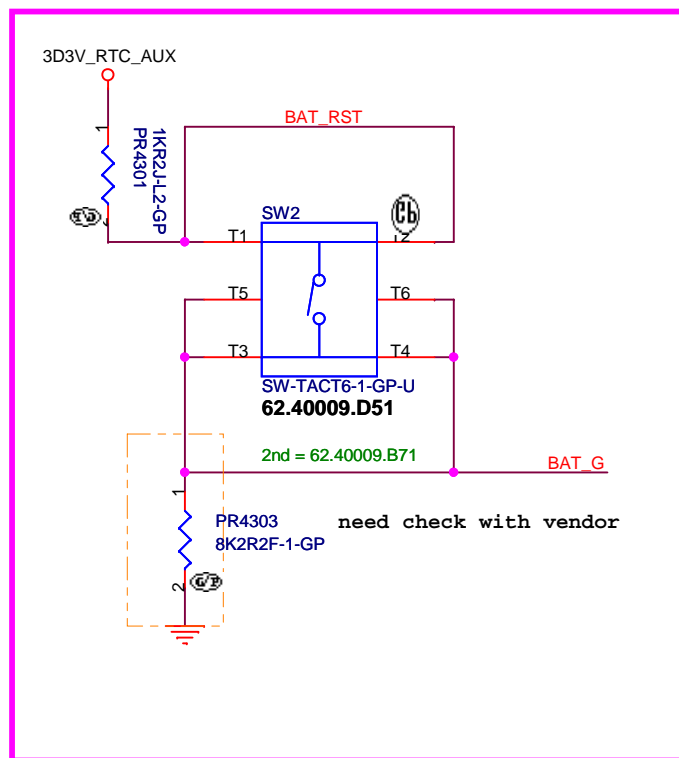
Rev

Date: Tuesday, April 15, 2014

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## DC IN connector



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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	1-15
2. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	16-30
3. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	31-45
4. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	46-60
5. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	61-75
6. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	76-90
7. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	91-105
8. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	106-120
9. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	121-135
10. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	136-150

**BATT CONN**

Size  
A4

Document Number
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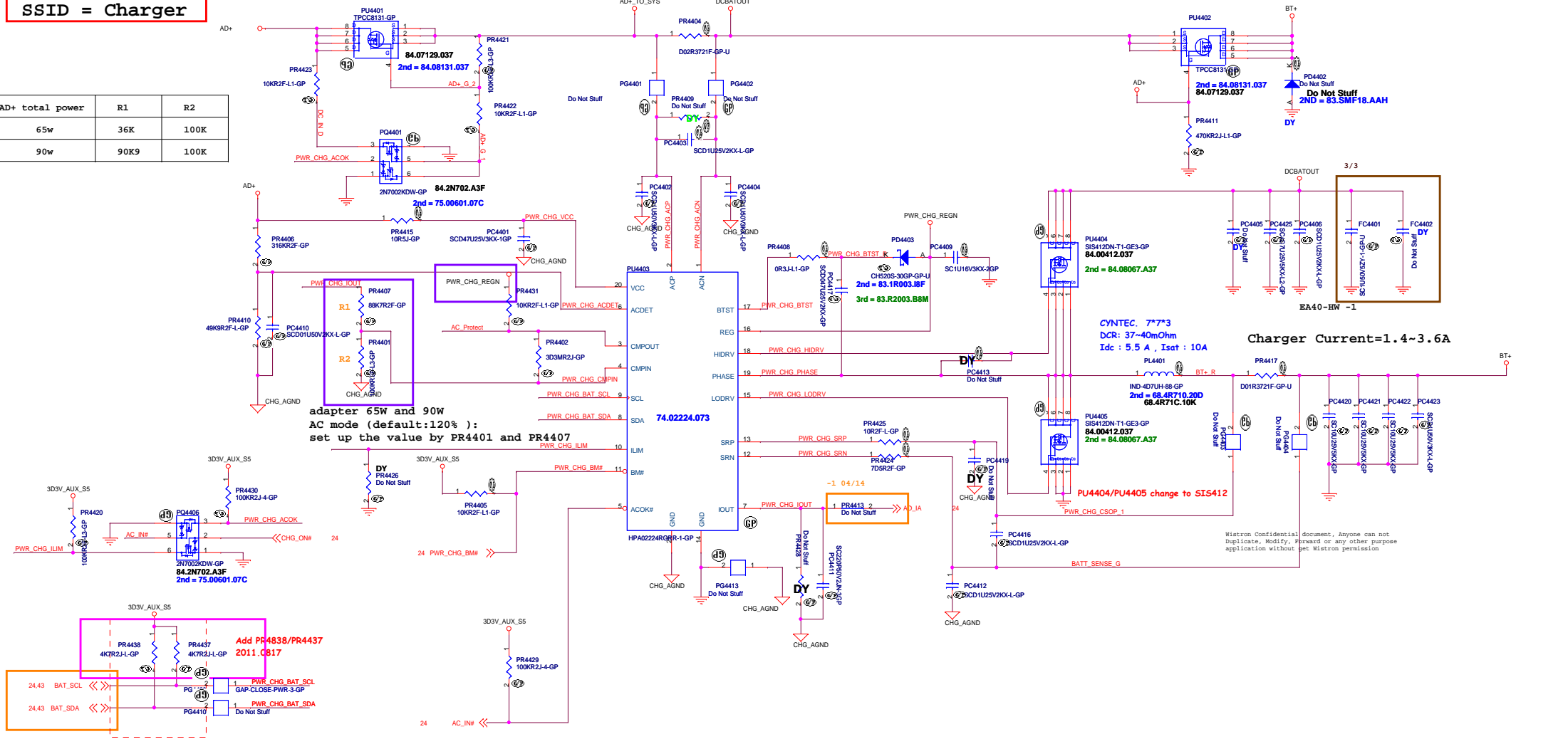
# MA30\_HB ULT

Rev  
2

Date: Tuesday, April 15, 2014

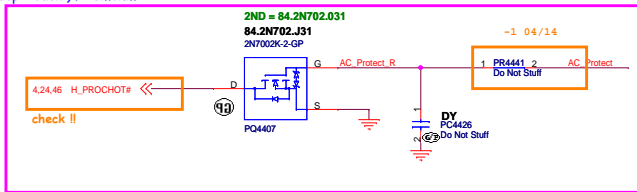
Sheet 43 of 102

AD+ total power	R1	R2
65w	36K	100K
90w	90K9	100K



AC adapter detect current :  

$$I_{ac} = 20 \times (V_{acp} - V_{acn}) / 10\text{mohm}$$

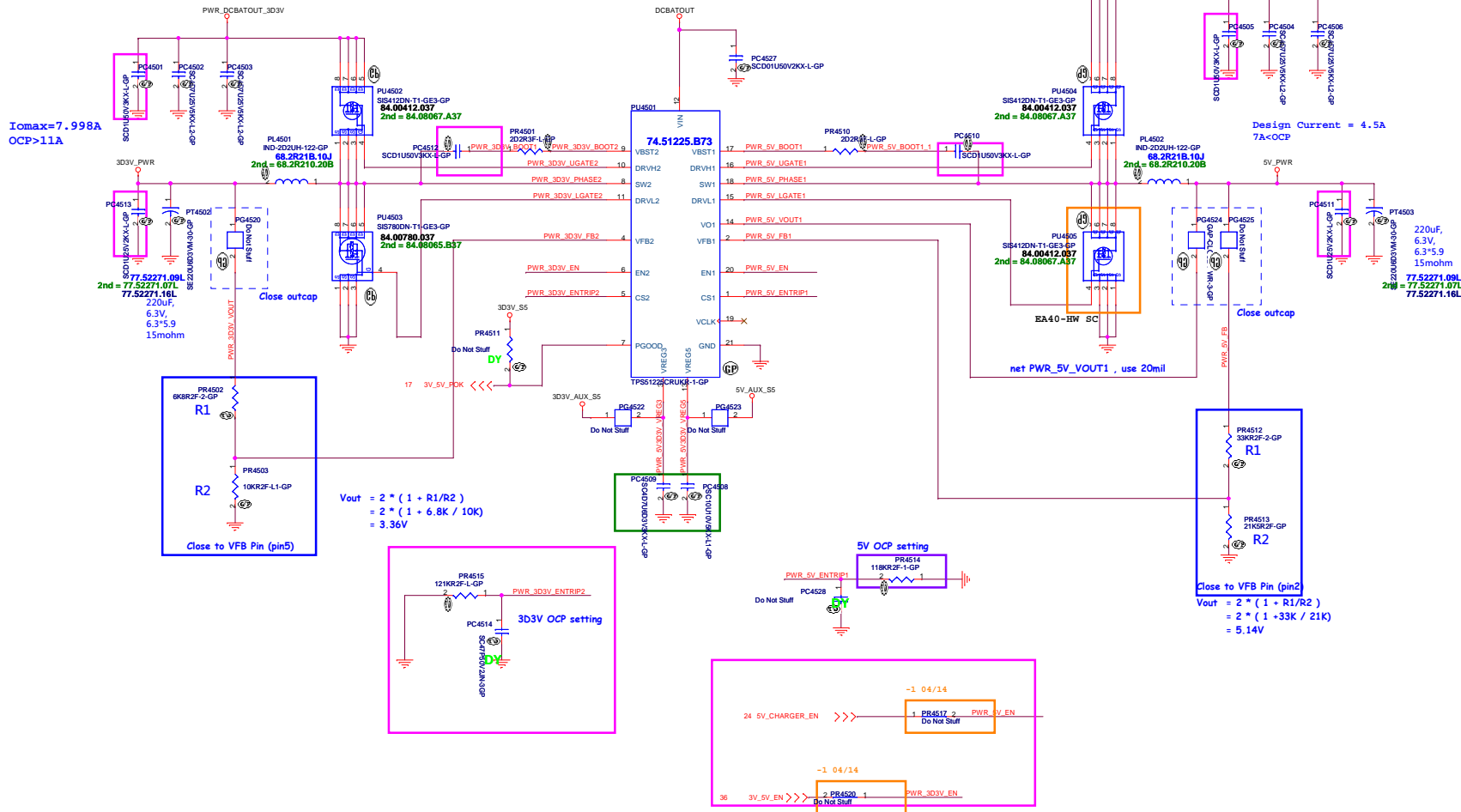
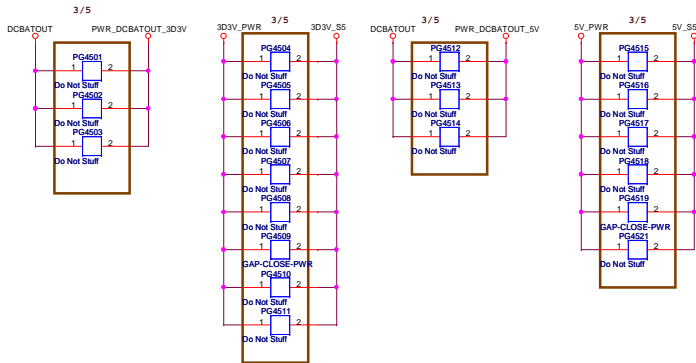


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Title			
<b>CHARGER BQ24737</b>			
Size	Document Number	Rev	
Custom	<b>MA30 HB ULT</b>	<b>SA</b>	
Date:	Tuesday, April 15, 2014	Sheet	44 of 102

```
SSID = PWR.Plane.Regulator_3p3v5v
```



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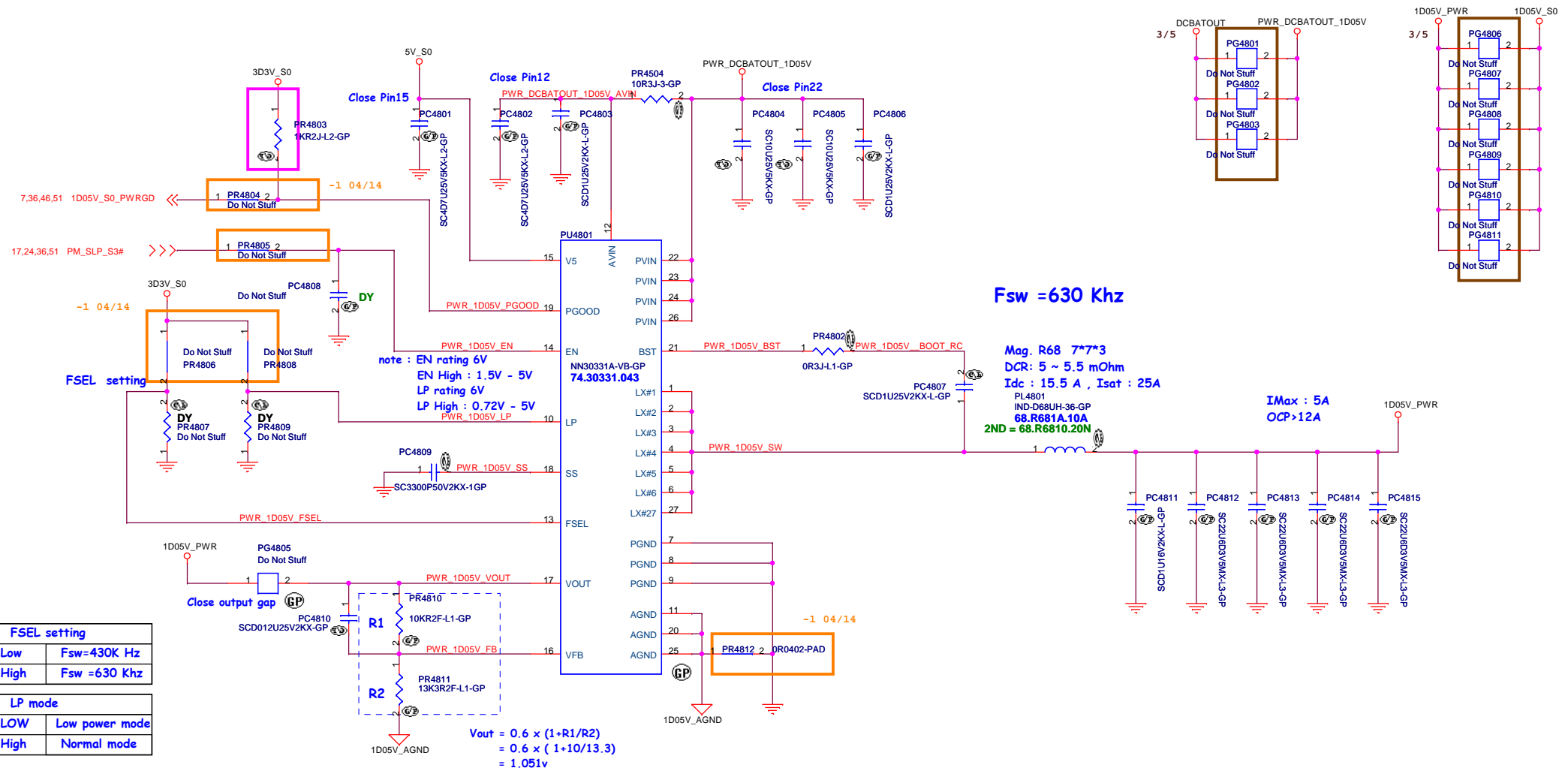
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Title			
TPS51225 5V/3D3V			
Size	Document Number	Rev	
Custom	MA30 HB ULT	SA	
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<p>Title</p>			
<p>TPS51622 CPUCORE(1/2)</p>			
<p>Size C</p>	<p>Document Number</p> <p>MA30 HB ULT</p>		<p>Rev</p> <p>2</p>
<p>Date</p>	<p>Tuesday, April 15, 2014</p>	<p>Sheet 46 of</p>	<p>102</p>



# NN30331 for 1D05V



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Title			
1D8V S0 SYW232			
Size	Document Number		Rev
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SYW232 for 1D5V\_S0

3D3V\_S5 3/5 3D3V\_PVDD\_PWR\_1D5V

PG5101 1 2 GAP-CLOSE-PWR

PC5104 SC1U10V2KX-L1-GP

PU5103 1 2 3 4 5 VIN VSS ON/OFF NC#4 VOUT

1D5V\_PWR

3/5 1D5V\_S0

PG5103 1 2 Do Not Stuff

7,36,46,48 1D05V\_S0\_PWRGD >>

17,24,36,48 PM\_SLP\_S3# >>

1D5V\_PWR\_EN

PC5105 Do Not Stuff

PC5106 SC1U10V2KX-L1-GP

PR5101 1 2 Do Not Stuff

PR5102 1 2 Do Not Stuff

PWR\_1D5V\_S0\_EN

PR5107 Do Not Stuff

S-1339D15-M5001-GP

Fix Vout=1.5V

Imax=300mA

OCP = 400mA

74.01339B3F

2nd = 74.70215.03F

Iomax=120mA

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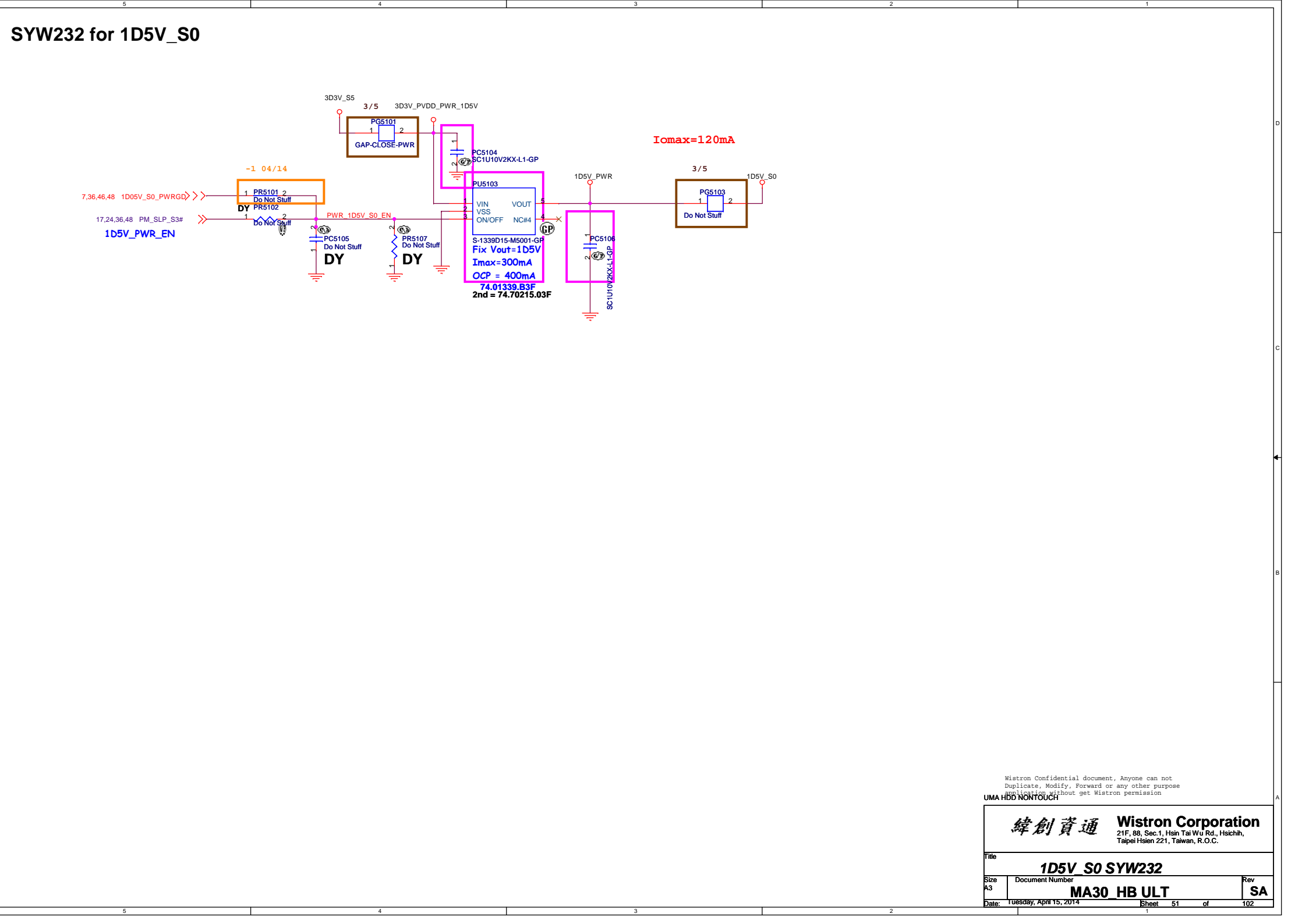
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Title 1D5V\_S0 SYW232

Size A3 Document Number MA30\_HB\_ULT Rev SA

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[illegible]

SYW232 for 1D5V\_S0

3D3V\_S5 3/5 3D3V\_PVDD\_PWR\_1D5V

PG5101 1 2 GAP-CLOSE-PWR

PC5104 SC1U10V2KX-L1-GP

PU5103 1 2 3 4 5 VIN VSS ON/OFF NC#4 VOUT

1D5V\_PWR

3/5 1D5V\_S0

PG5103 1 2 Do Not Stuff

7,36,46,48 1D05V\_S0\_PWRGD >>

17,24,36,48 PM\_SLP\_S3# >>

1D5V\_PWR\_EN

PC5105 Do Not Stuff

PC5106 SC1U10V2KX-L1-GP

PR5107 Do Not Stuff

PR5101 1 2 Do Not Stuff

PR5102 1 2 Do Not Stuff

PWR\_1D5V\_S0\_EN

DY

DY

S-1339D15-M5001-GP

Fix Vout=1.5V

Imax=300mA

OCP = 400mA

74.01339B3F

2nd = 74.70215.03F

Iomax=120mA

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Title 1D5V\_S0 SYW232

Size A3 Document Number MA30\_HB ULT Rev SA

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SYW232 for 1D5V\_S0

3D3V\_S5 3/5 3D3V\_PVDD\_PWR\_1D5V

PG5101 1 2 GAP-CLOSE-PWR

PC5104 SC1U10V2KX-L1-GP

PU5103 1 2 3 4 5 VIN VSS ON/OFF NC#4 VOUT

S-1339D15-M5001-GP Fix Vout=1.5V Imax=300mA OCP = 400mA 74.01339B3F 2nd = 74.70215.03F

PC5106 SC1U10V2KX-L1-GP

1D5V\_PWR

3/5 1D5V\_S0

PG5103 1 2 Do Not Stuff

7,36,46,48 1D05V\_S0\_PWRGD >>

17,24,36,48 PM\_SLP\_S3# >>

1D5V\_PWR\_EN

PC5105 Do Not Stuff

PR5107 Do Not Stuff

PC5105 Do Not Stuff

PR5102 Do Not Stuff

PR5101 1 2 Do Not Stuff

PC5105 Do Not Stuff

PR5107 Do Not Stuff

PC5106 SC1U10V2KX-L1-GP

1D5V\_PWR

3/5 1D5V\_S0

PG5103 1 2 Do Not Stuff

Iomax=120mA

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1D5V\_S0 SYW232

MA30\_HB ULT

SA

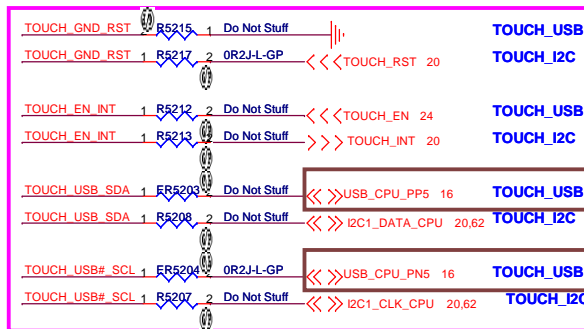
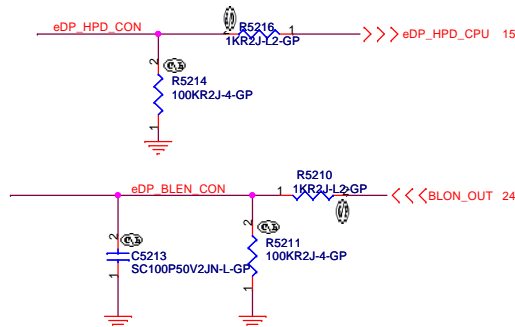
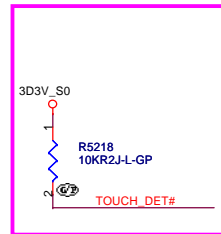
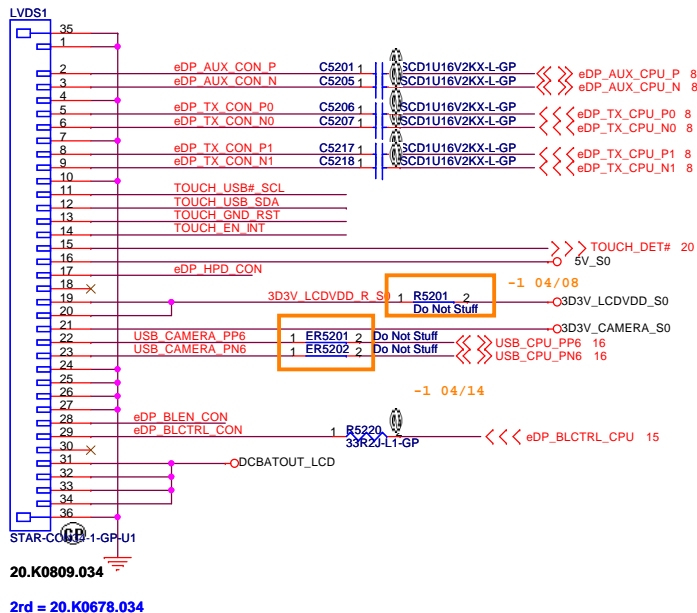
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Document Number

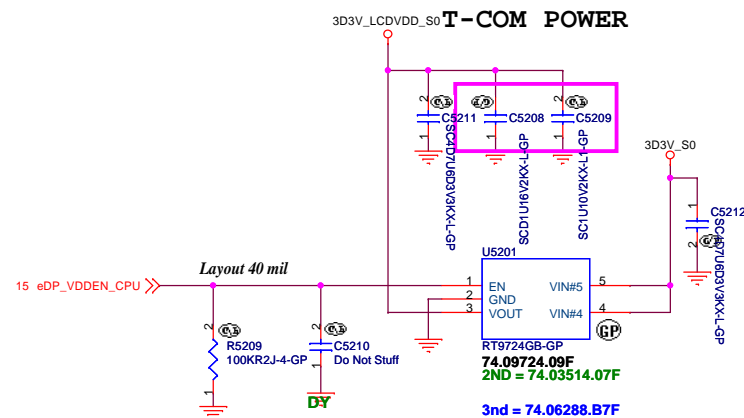
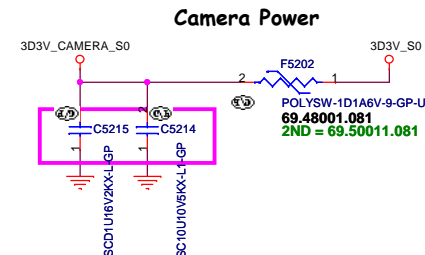
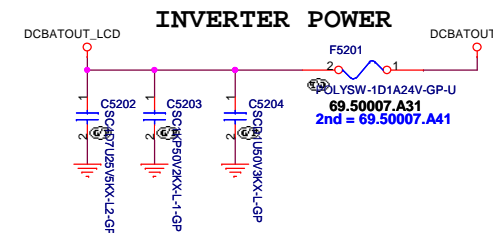
Date: Tuesday, April 15, 2014

Sheet 51 of 102

SSID = VIDEO



2/19



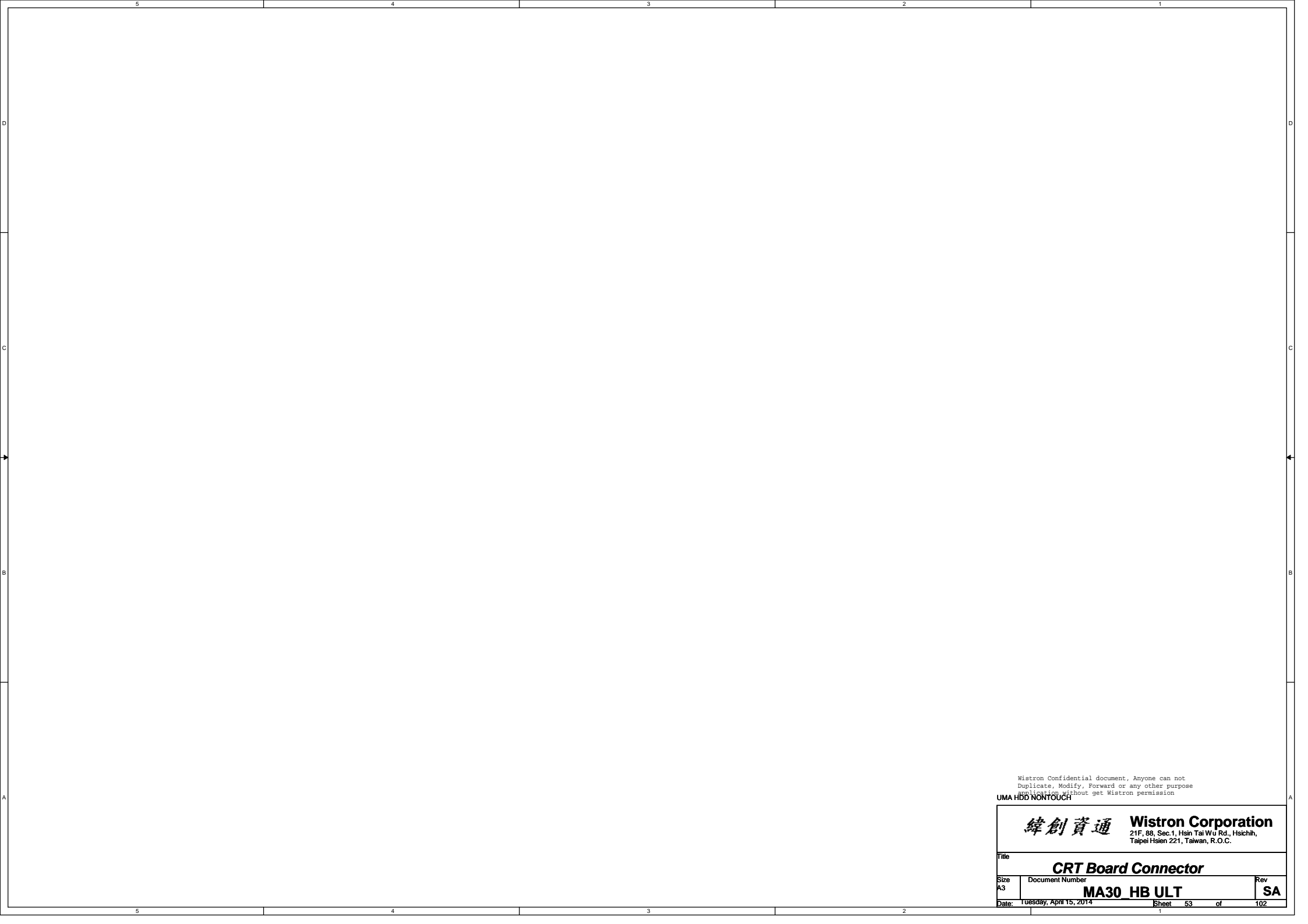
EDP connector

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EDP Connector			
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Date: Tuesday, April 15, 2014	Sheet 52	of	102



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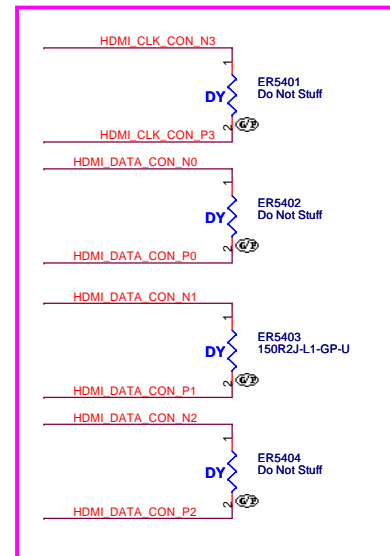
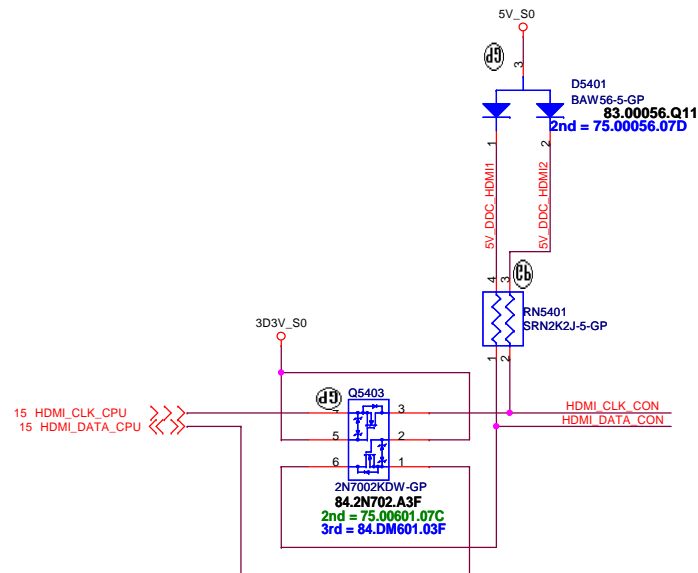
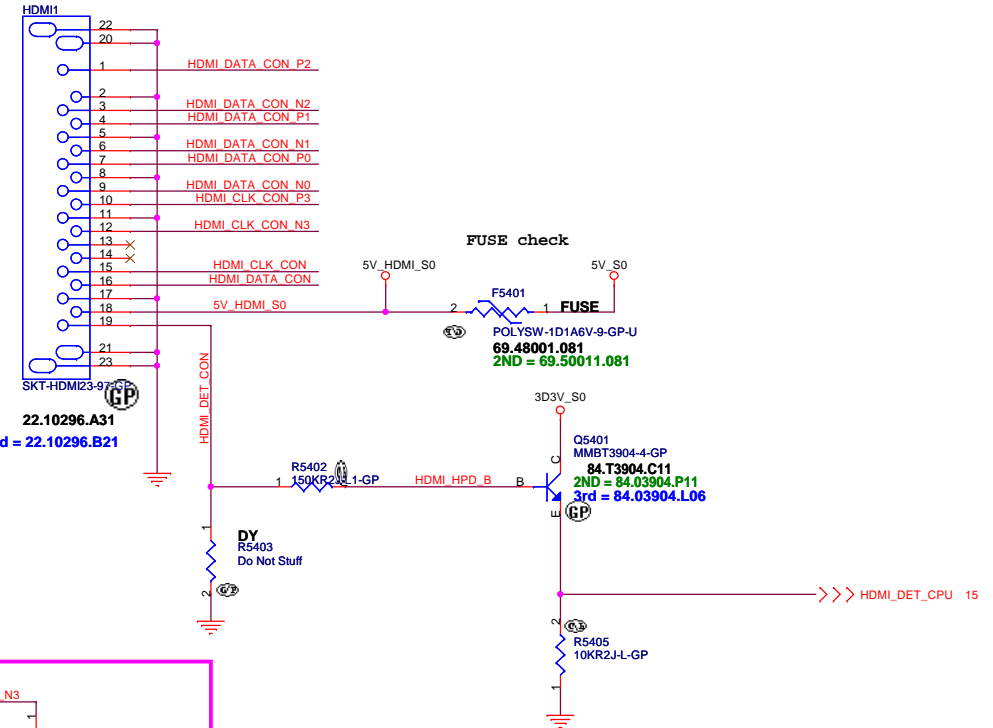
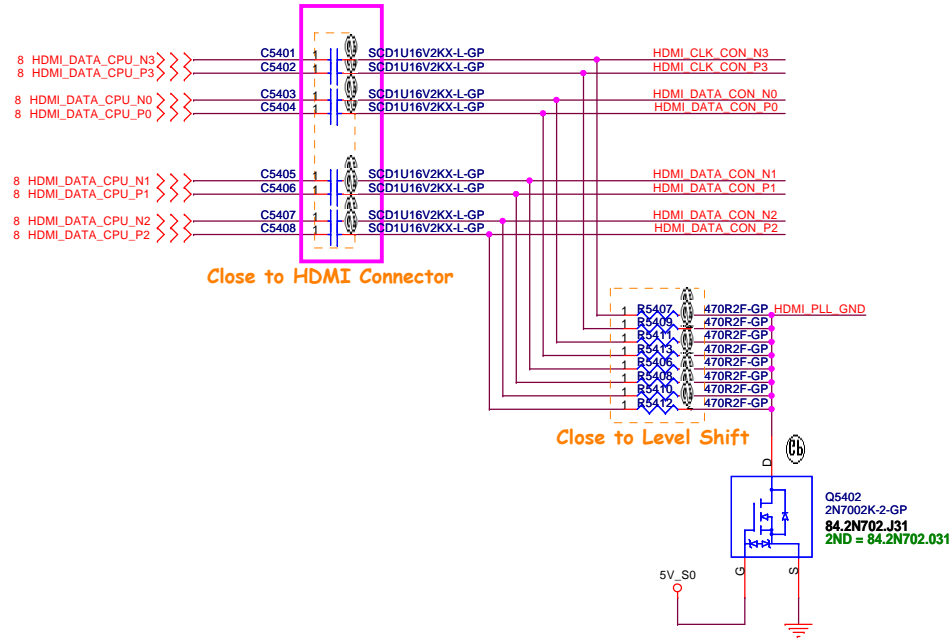
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Title			
CRT Board Connector			
Size	Document Number		Rev
A3	MA30 HB ULT		SA
Date:	Tuesday, April 15, 2014		Sheet 53 of 102

SSID = VIDEO

# HDMI Level Shifter & CONNECTOR

## HDMI CONN

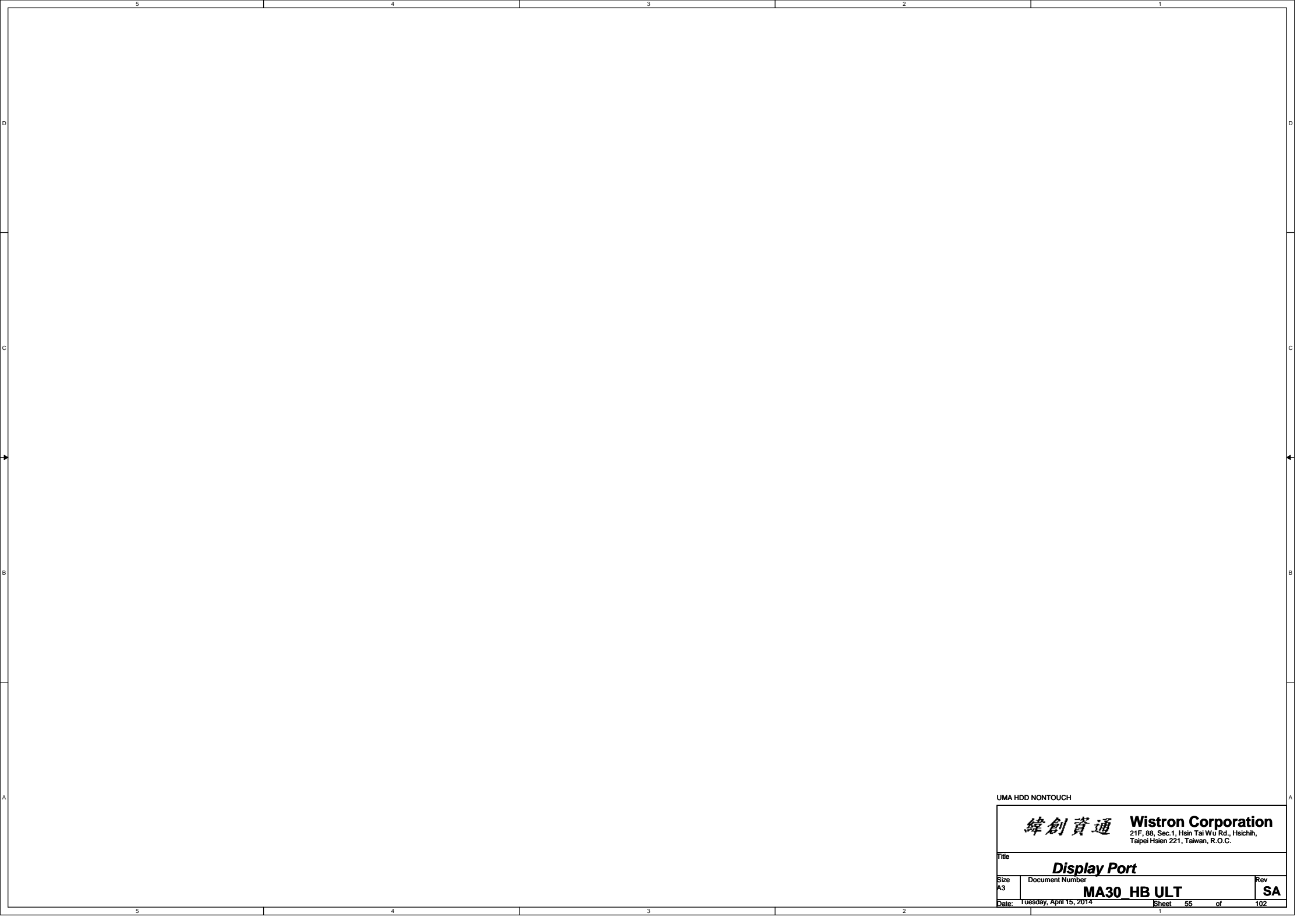


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Title			HDMI Level Shifter/Connector	
Size	Document Number	Rev		
A3	MA30_HB_UL	SA		
Date:	1 Tuesday, April 15, 2014	Sheet	54	of 102

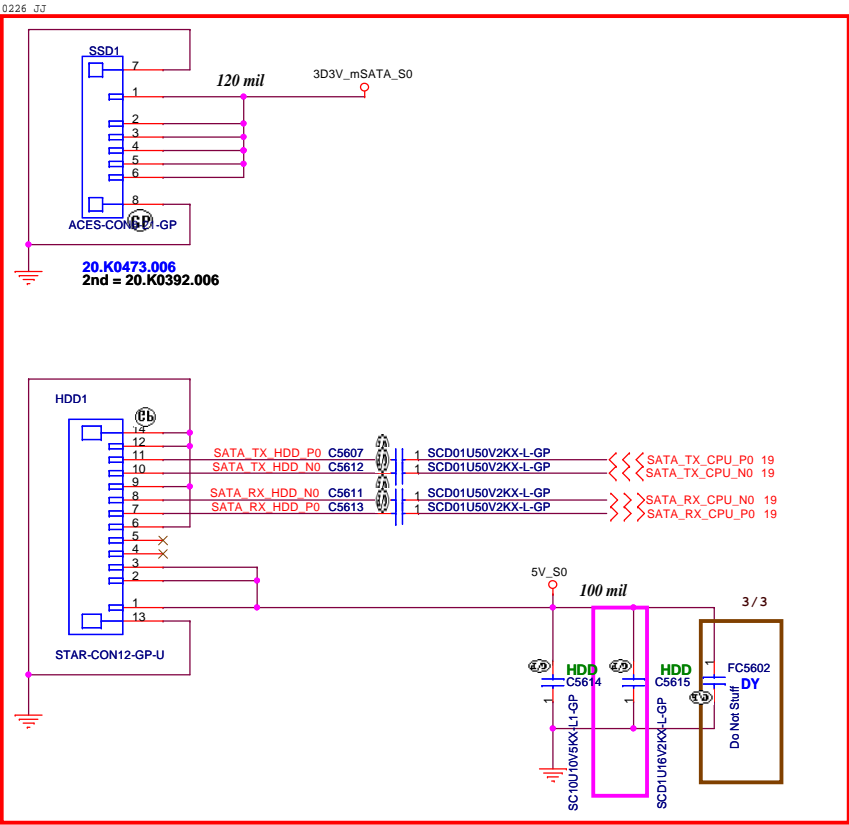


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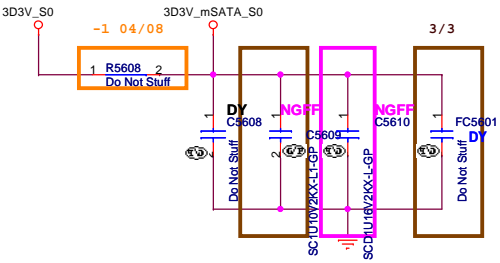
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Title			
<b>Display Port</b>			
Size	Document Number		Rev
A3	<b>MA30_HB_ULT</b>		<b>SA</b>
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SSID = SATA

# SATA HDD Connector



AC coupling caps near connector<100 mils  
Delay HDD power off timing for 800ms~900ms after SATA controller shut down.



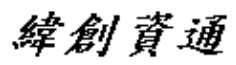
# NGFF SSD Connector



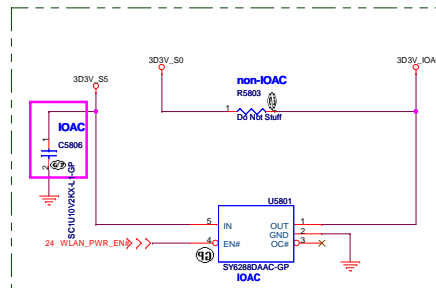
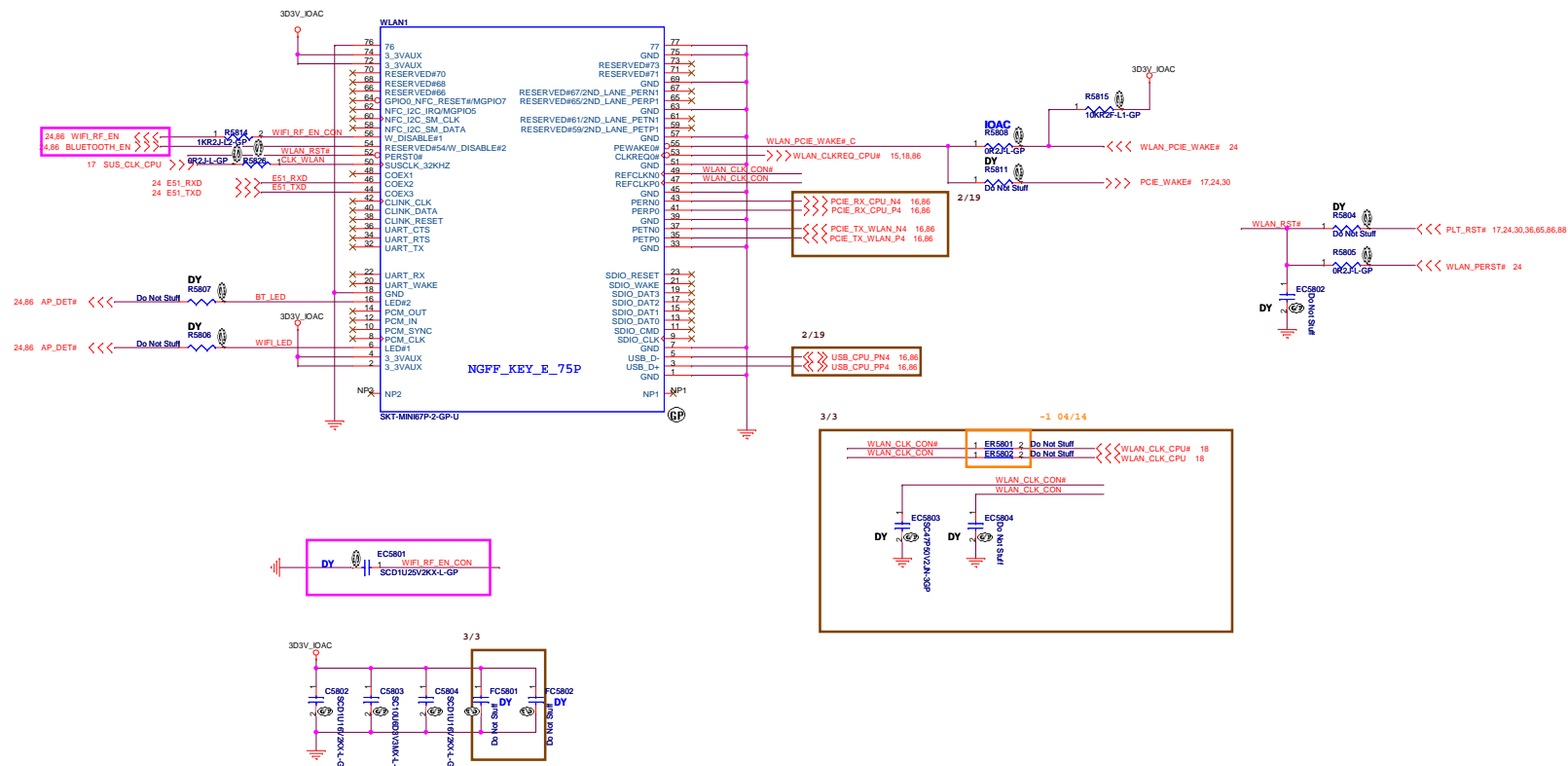
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Title		
<b>E-SATA</b>		
Size A4	Document Number <b>EA40 HB ULT</b>	Rev <b>2</b>
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# SSID = Wireless Mini Card Connector(802.11a/b/g/n)



Debug Card Circuit

SSID = Wireless

# Mini Card Connector(mSATA)

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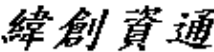
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>WWAN CONN</b>		
Size A4	Document Number <b>MA30 HB ULT</b>	Rev <b>2</b>
Date: Tuesday, April 15, 2014		Sheet 59 of 102

SSID = mSATA

# Mini Card Connector(mSATA)

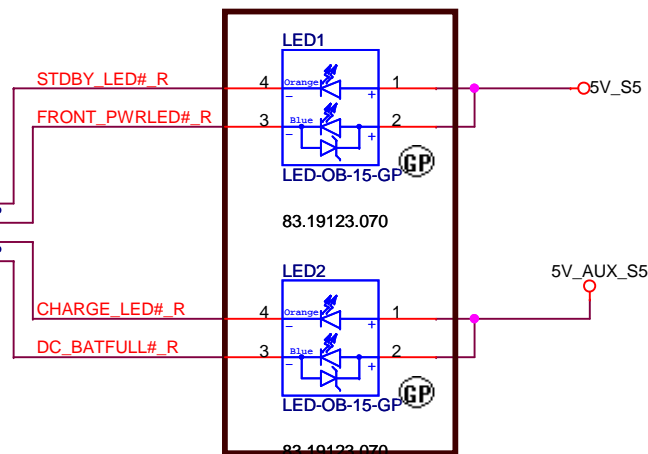
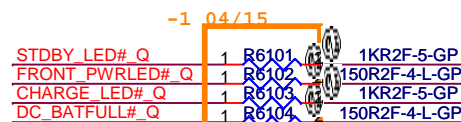
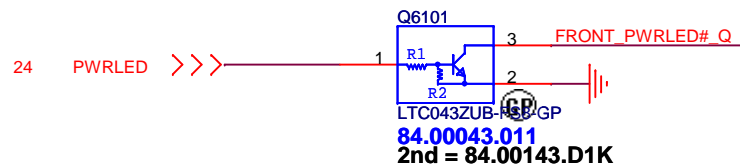
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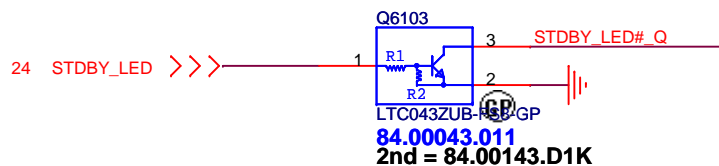
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>mSATA Connector</b>			
Size A4	Document Number <b>MA30 HB ULT</b>		Rev <b>2</b>
Date: Tuesday, April 15, 2014		Sheet 60	of 102

SSID = User.Interface

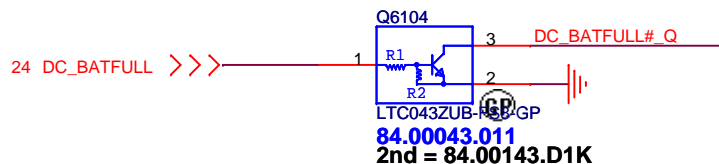
## Power button\_LED



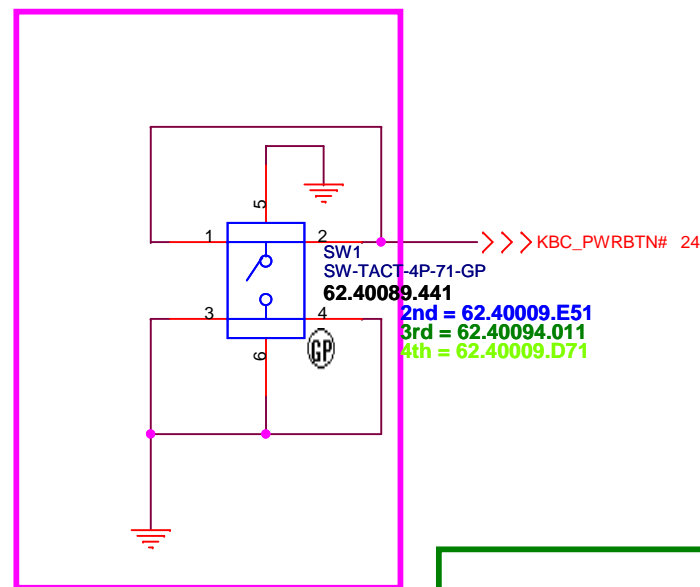
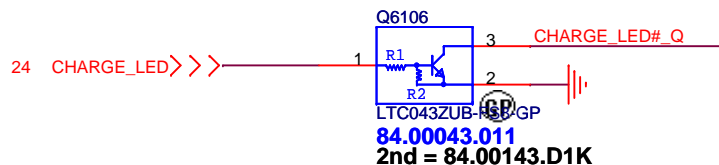
## Power STDBY\_LED



## Battery LED2 (DC\_BATFULL)



## Battery LED1 (CHARGE)



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Title

LED Bard/Power Button

Size  
A4

Document Number

MA30 HB ULT

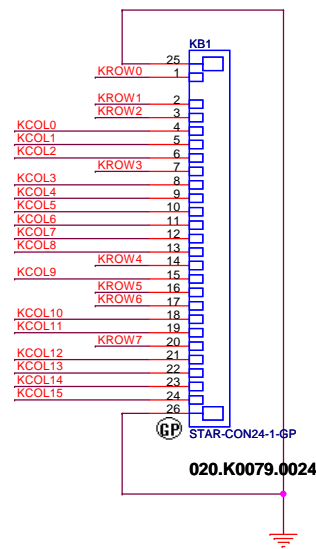
Rev  
SA

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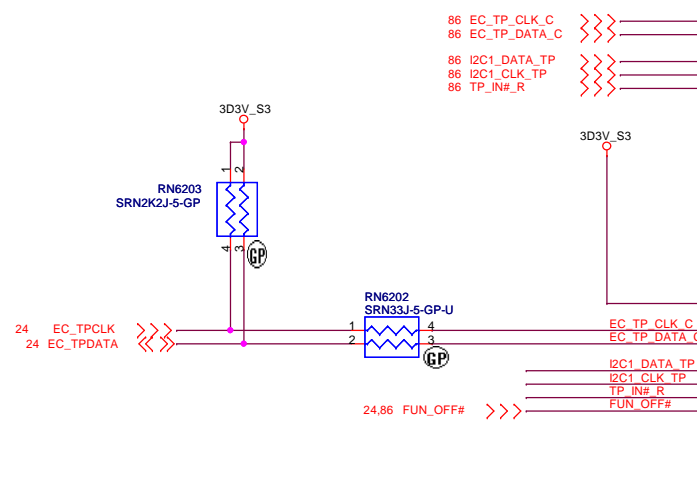
SSID = Key Board CN & TP CN

24,86 KROW[0..7] >>> >>>  
24,86 KCOL[0..15] >>> >>>

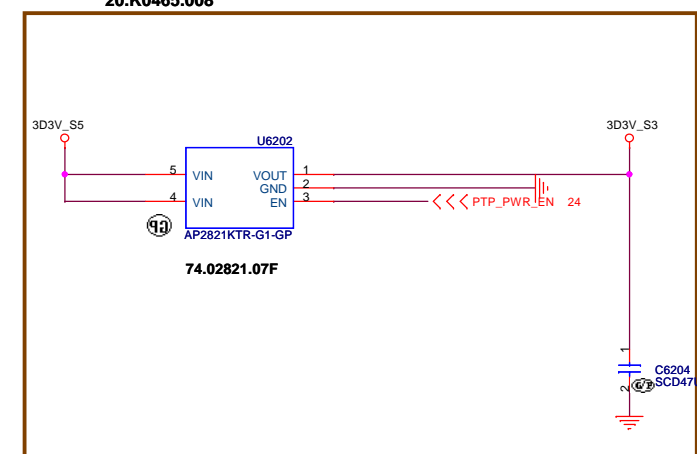
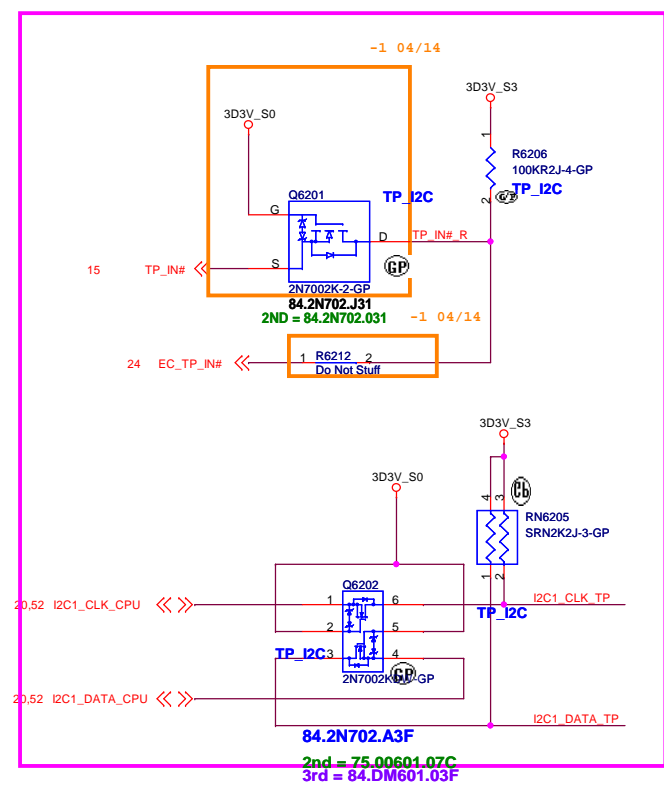
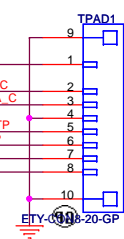


MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1  
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 **K/B** 1



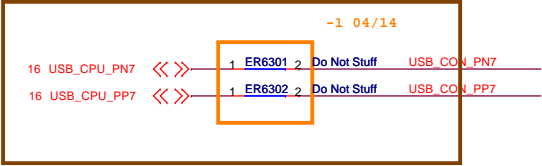
TOUCH PAD



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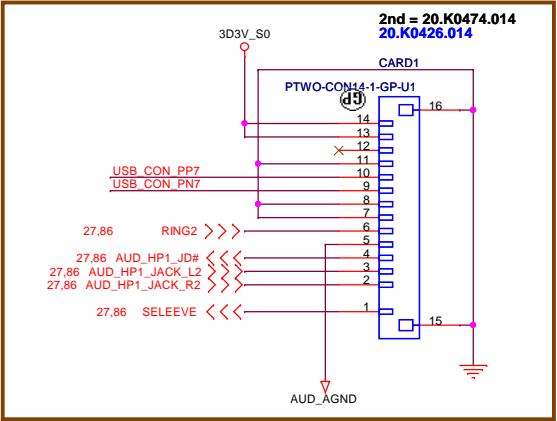
UMA HDD NONTOUCH

2/19



86 USB\_CON\_PP7 << >> \_\_\_\_\_

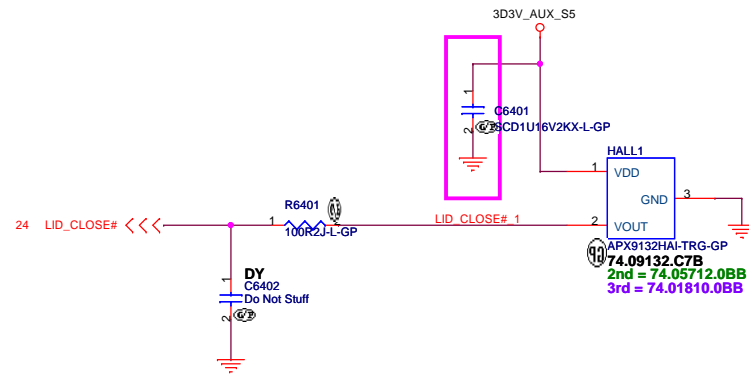
86 USB\_CON\_PN7 << >> \_\_\_\_\_



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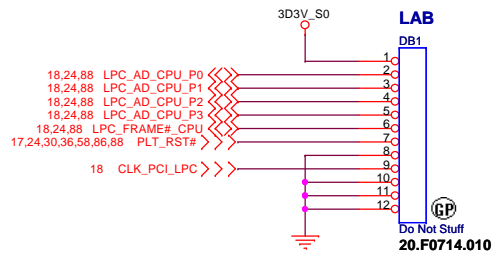
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Title					
<b>IO Board Connector</b>					
Size	Document Number				Rev
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Title	
Hall Sensor	
Size	Document Number
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Title		
<b>Dubug connector</b>		
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(Blanking)

# Free Fall Sensor

## Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

SDO="H"; address="3Ah"  
\*SDO="L"; address="38h"

\*CS="H"; mode="I2C"  
CS="L"; mode="SPI"

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Title

**G Sensor**

Size  
A

Document Number

**MA30 HB ULT**

Rev

**2**

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Title			
<b>Thunderbolt (1/5)</b>			
Size Custom	Document Number		Rev
	<b>MA30 HB ULT</b>		<b>2</b>
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Title			
Thunderbolt (2/5)			
Size	Document Number		Rev
Custom	MA30 HB ULT		2
Date:	Tuesday, April 15, 2014		
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5	4	3	2	1

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Title

Thunderbolt (3/5)

Size Custom

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MA30 HB ULT

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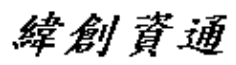
Rev 2



5	4	3	2	1
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Title <b>Thunderbolt (5/5)</b>		
Size A4	Document Number <b>MA30 HB ULT</b>	Rev <b>2</b>
Date: Tuesday, April 15, 2014		Sheet 72 of 102



5	4	3	2	1
D				D
C				C
B				B
A				A

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GPU (POWER/GND)

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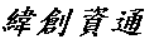
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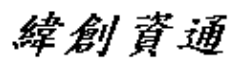
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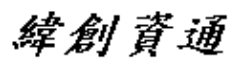
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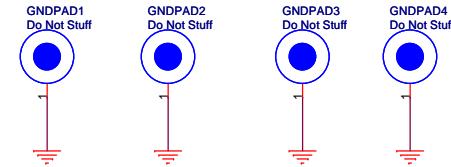
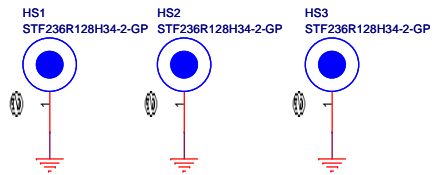
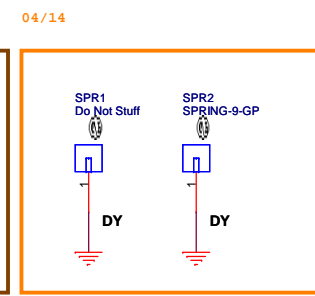
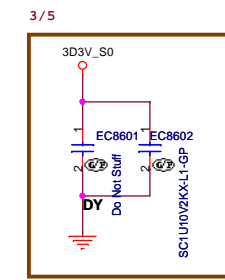
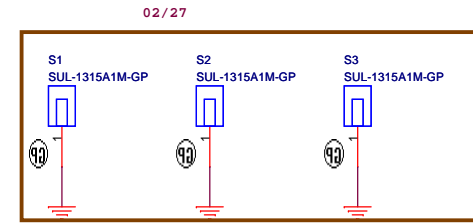
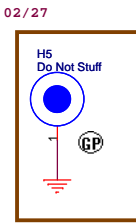
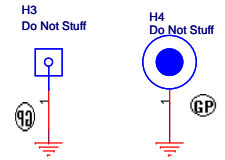
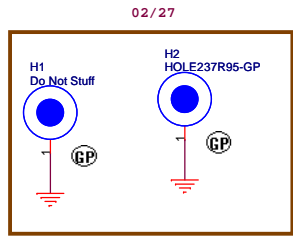
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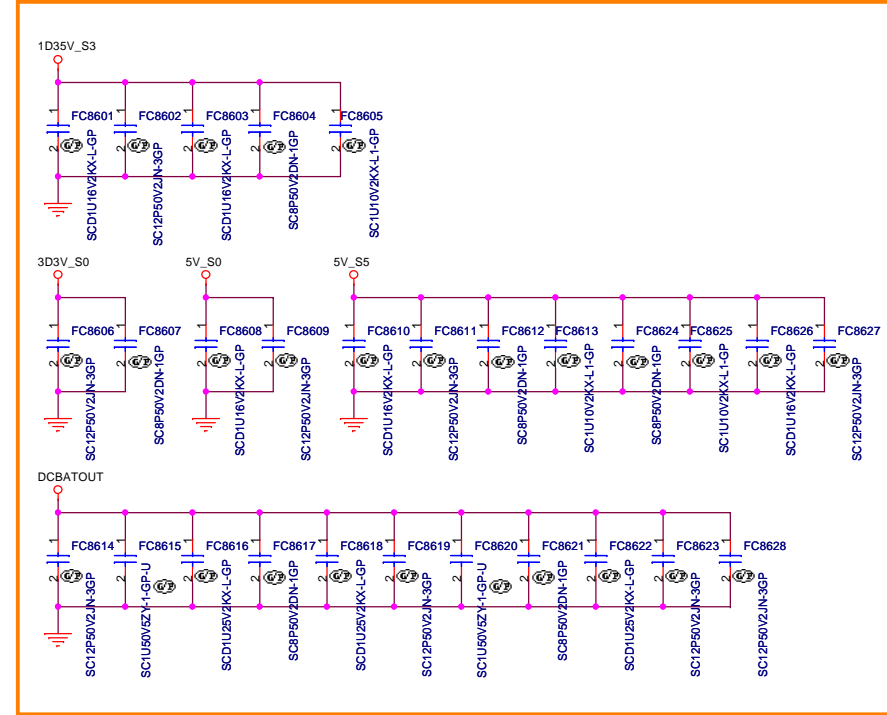
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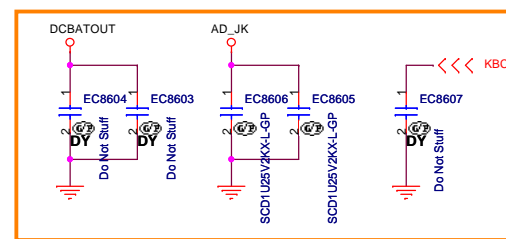
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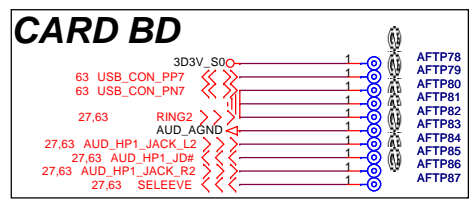
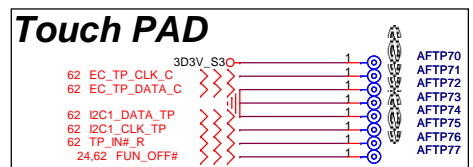
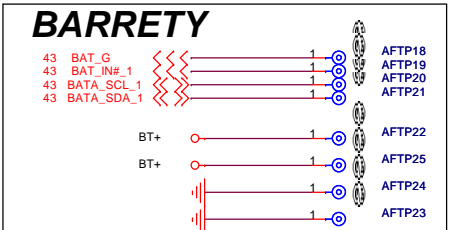
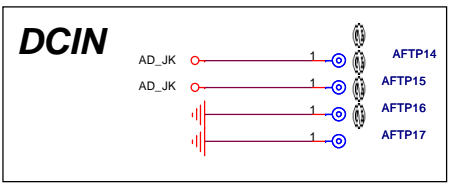
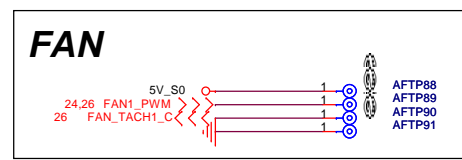
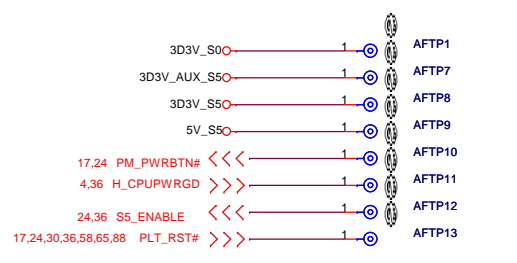


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**Check test point** Test Point放在Dimm Door打開可量測處



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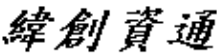




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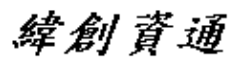
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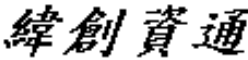
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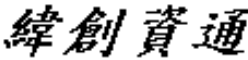
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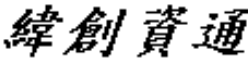
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Inter LAN WG1217LM

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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 <sup>1</sup>	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# <sup>1</sup>	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 <sup>1</sup>	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# <sup>1</sup>	O	System	18	HOOK7	DBR# <sup>1</sup>	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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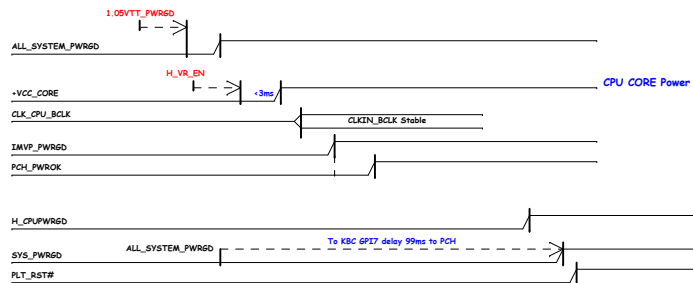
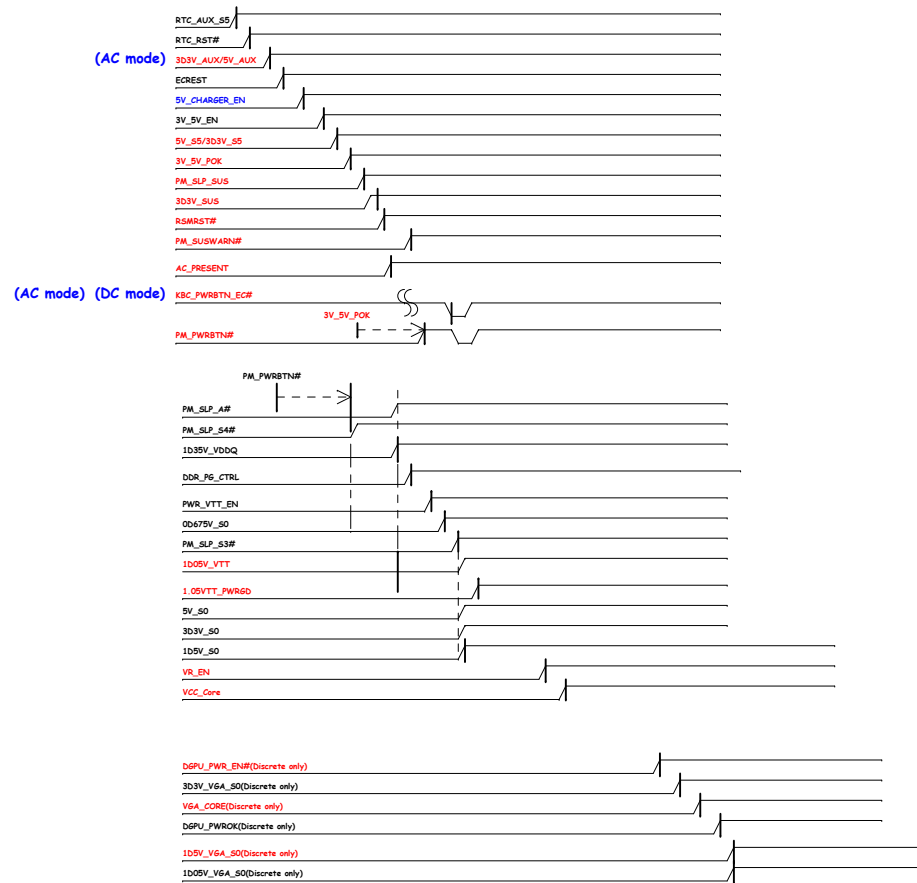
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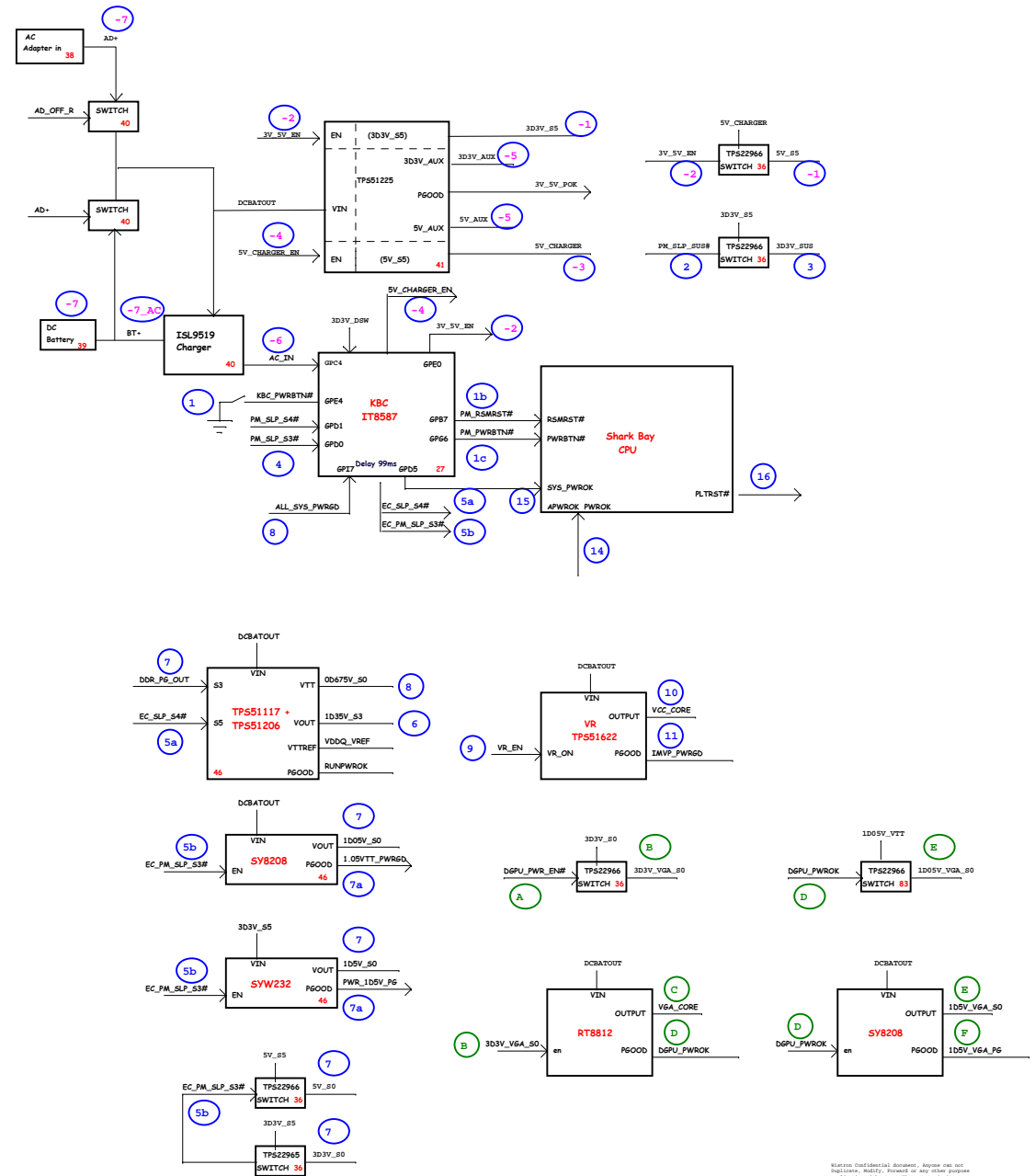
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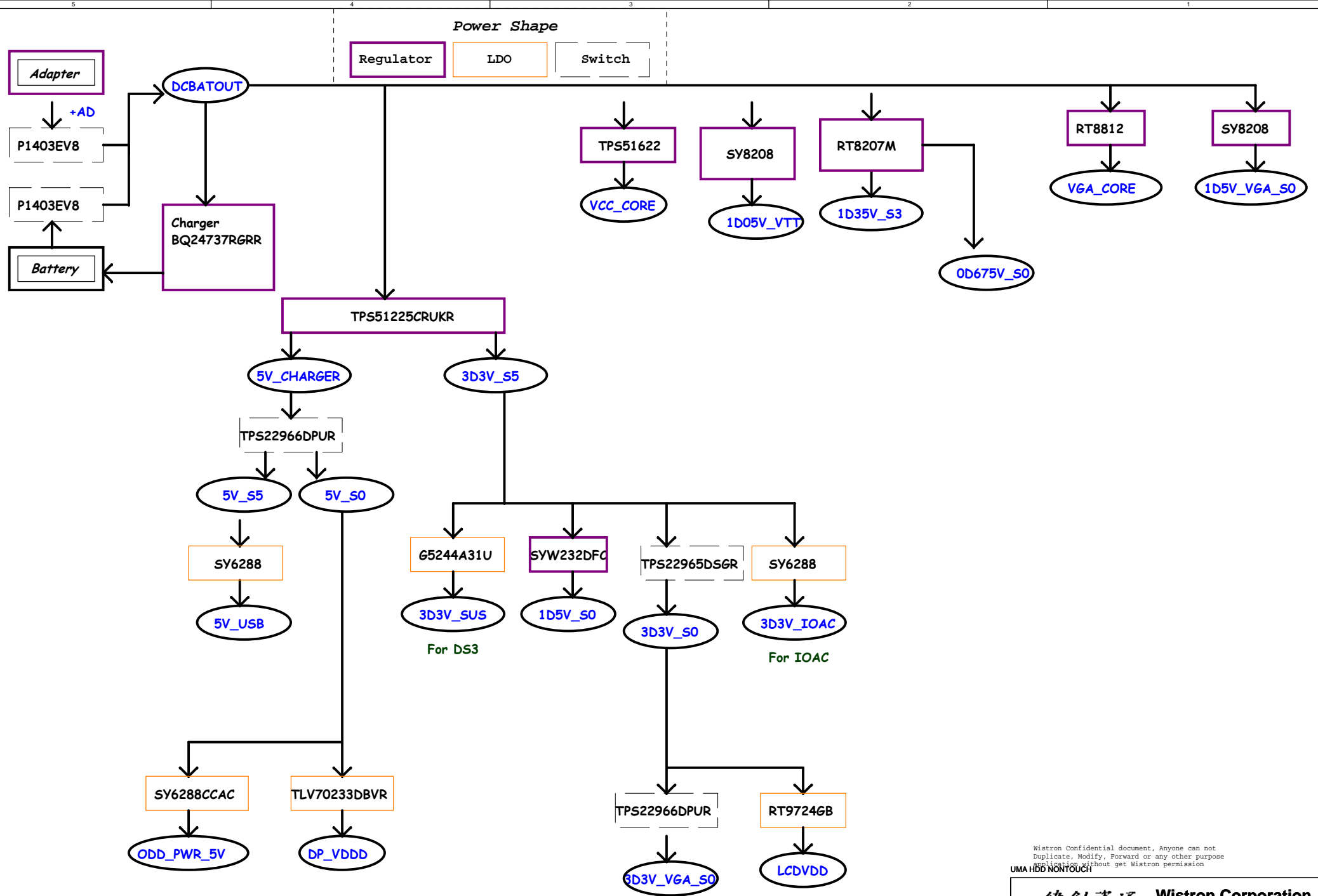
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## Intel-Power Up Sequence



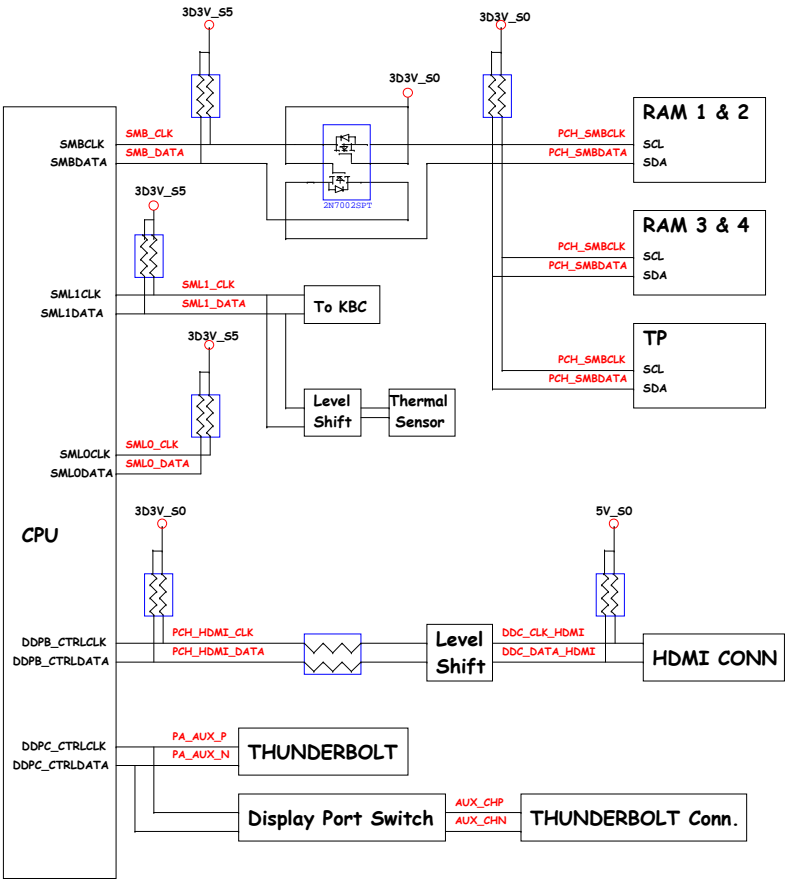
## SHARK BAY POWER UP SEQUENCE DIAGRAM



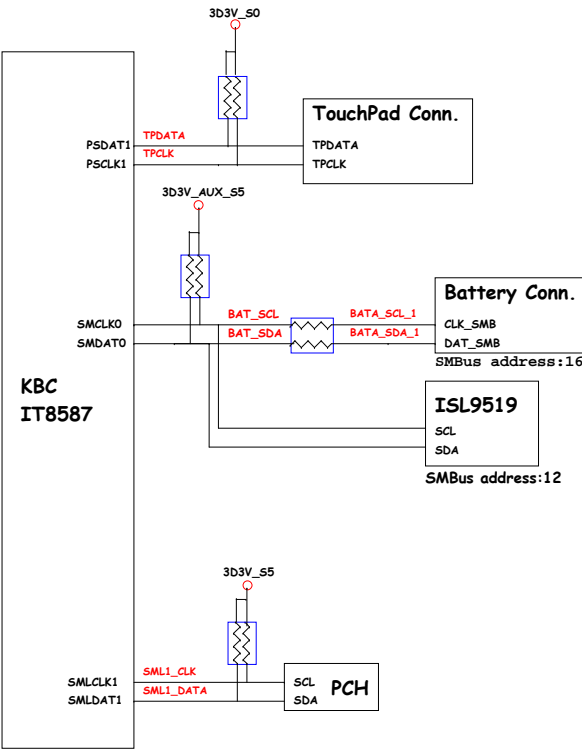


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PCH SMBus Block Diagram



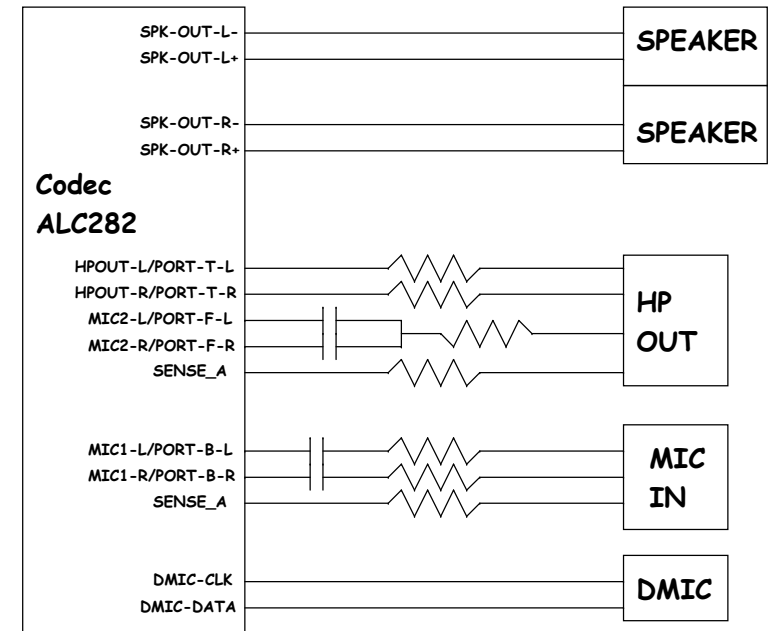
KBC SMBus Block Diagram



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<b>SMBUS BLOCK DIAGRAM</b>			
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### Audio Block Diagram



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